First Test Measurements of a 64k pixel readout chip working in single photon counting mode

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On behalf of the Medipix2 Collaboration*

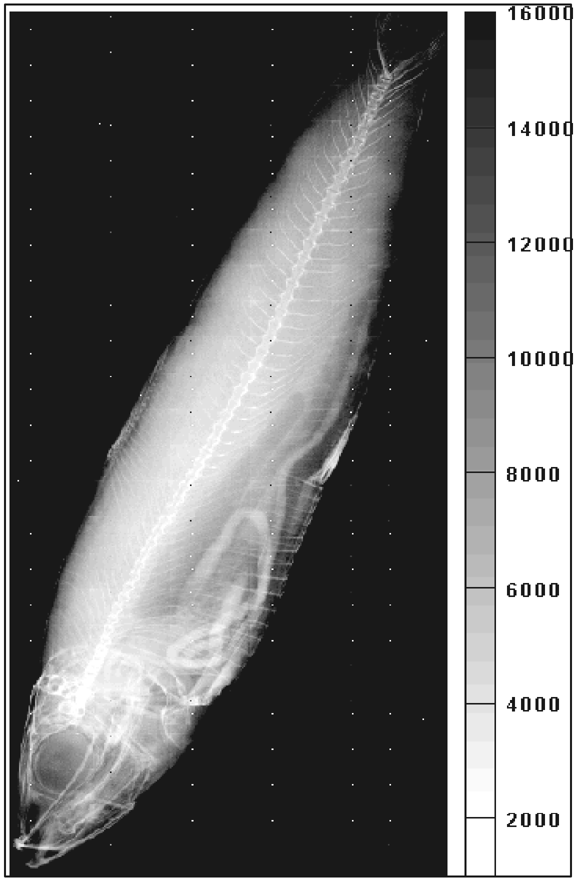
(Special thanks to X. Llopart)

*** See: http://medipix.web.cern.ch/MEDIPIX/**

Outline

- Introduction
- Motivation for the chip design
- The Medipix2 pixel cell
- The Medipix2 chip architecture
- Electrical measurements
- Conclusions
- Future work

Medipix1 image of a sardine



X-ray tube
Mo target
30 µm Mo filter
25 kV
5 mAs
50 cm from source
Raw data

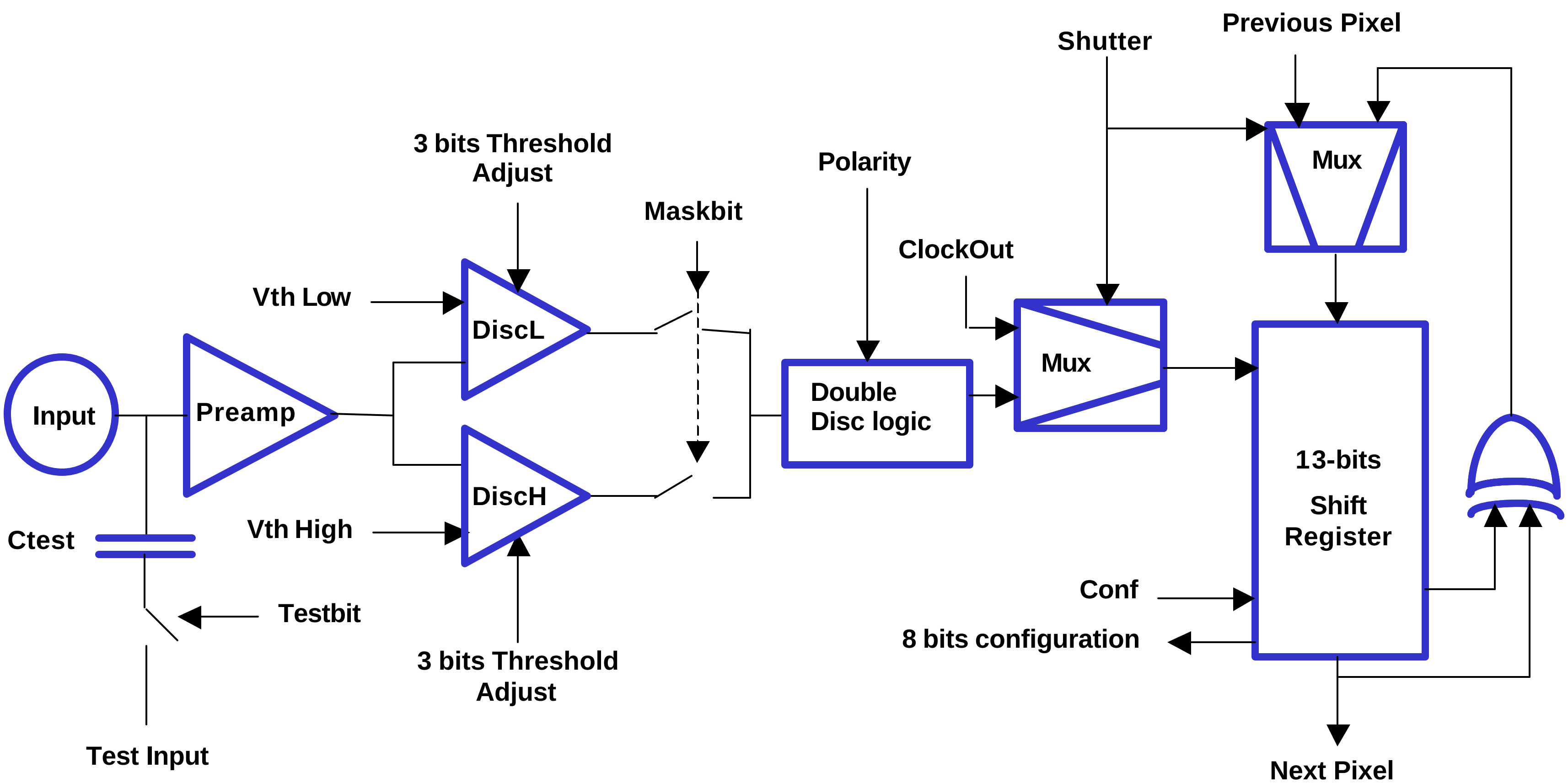
Motivations

- **Develop a single photon counting chip competitive in spatial resolution with film-screen systems**
- **Many high-Z detector materials trap holes – design front-end sensitive to both electron and hole collection**
- **Add 2 levels of discrimination to begin to study spectroscopic behaviour**
- **3-side buttable chip was required**
- **Deep sub-micron CMOS (0.25μm) was available and well characterized.**

Characteristics of Medipix2 Chip

- Square pixel size of 55 µm
- Sensitive to positive or negative input charge
- Pixel by pixel detector leakage current compensation
- Window in energy as precise as possible
- 13-bit counter per pixel
- Count rates of 1 MHz/pixel (0.33 GHz/mm^2)
- 256 x 256 pixels
- 3-side buttable
- serial or parallel I/O
- 9 special pixels with analog readout

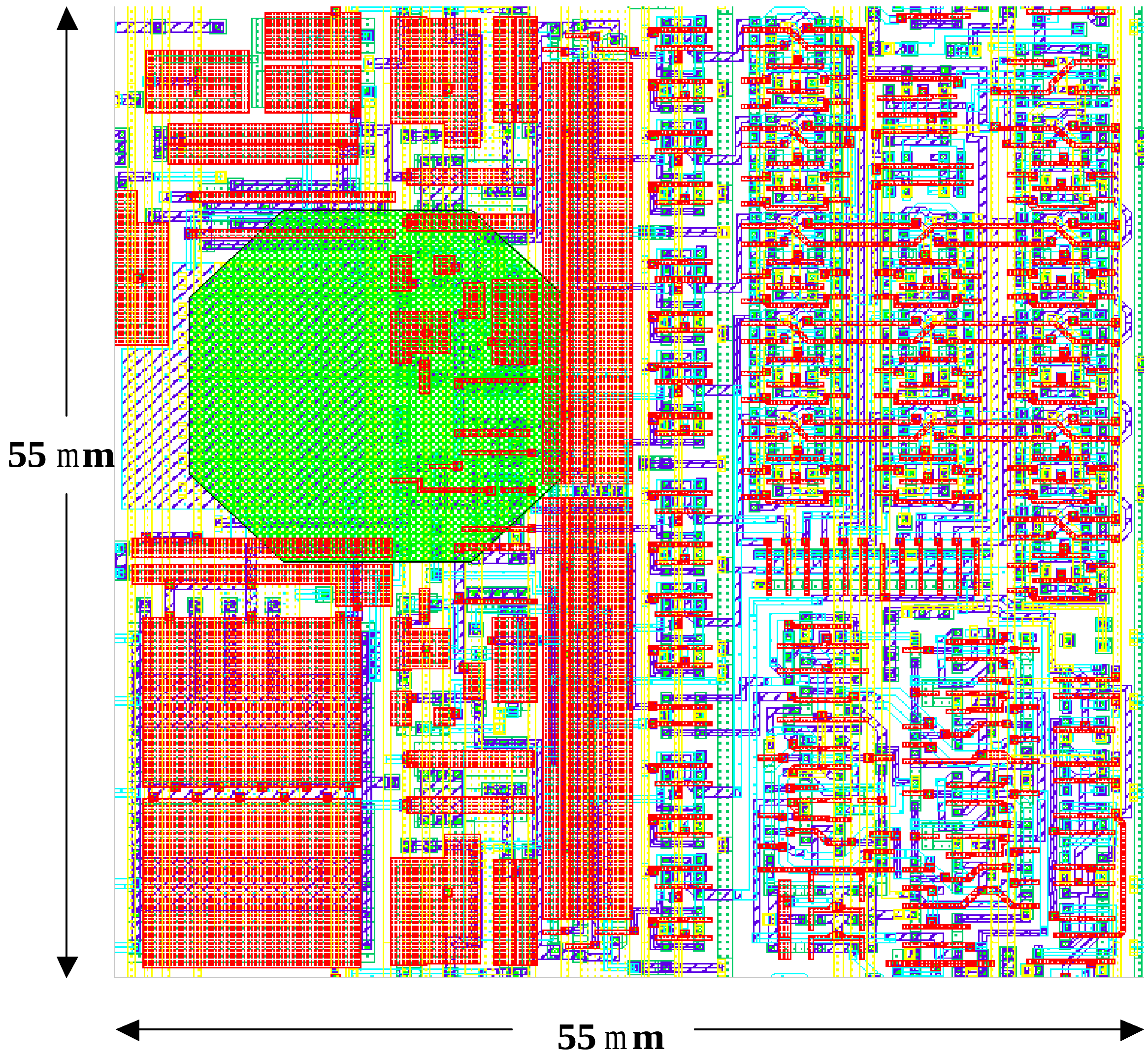
Medipix2 Pixel Cell



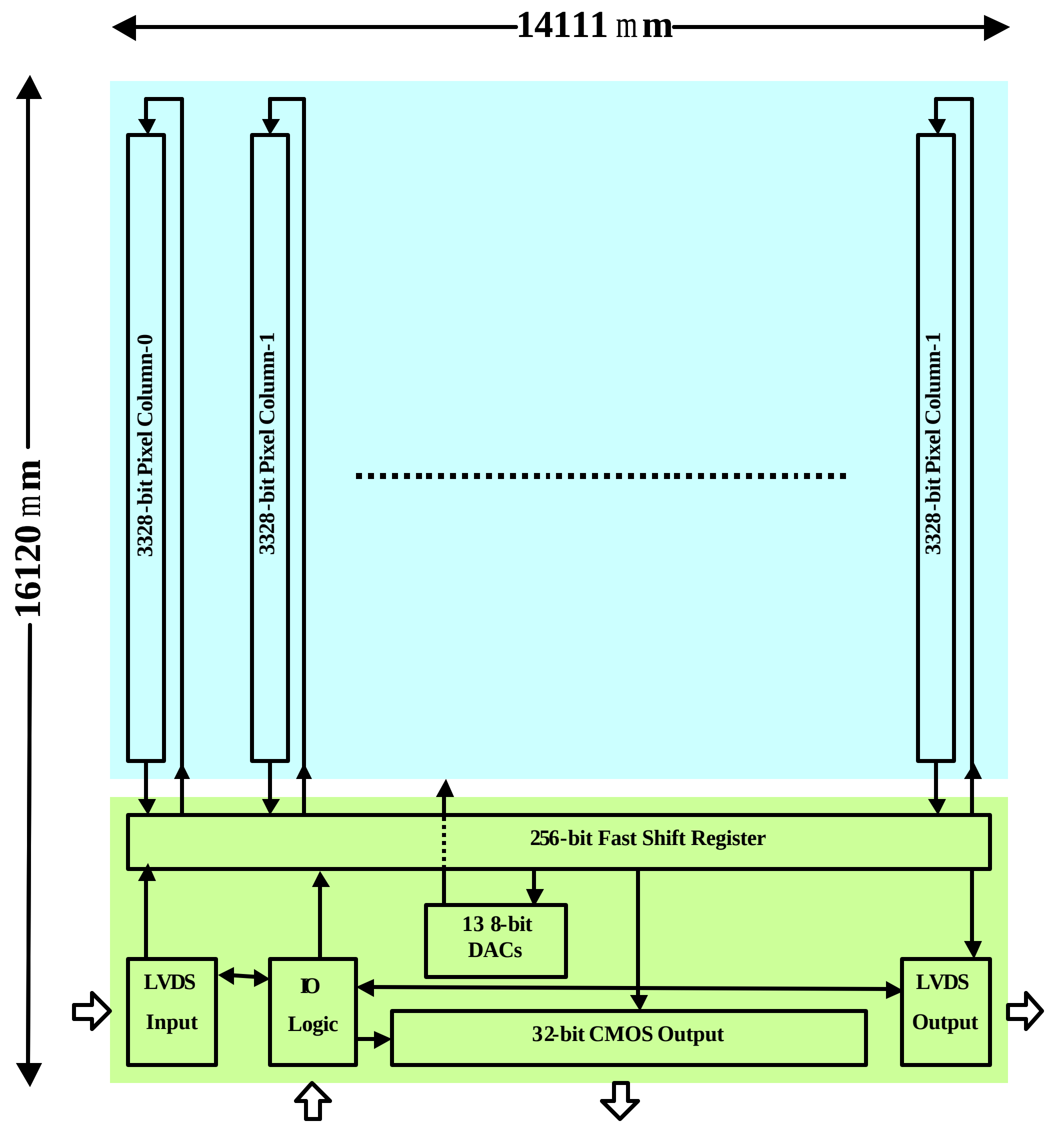
Analog

Digital

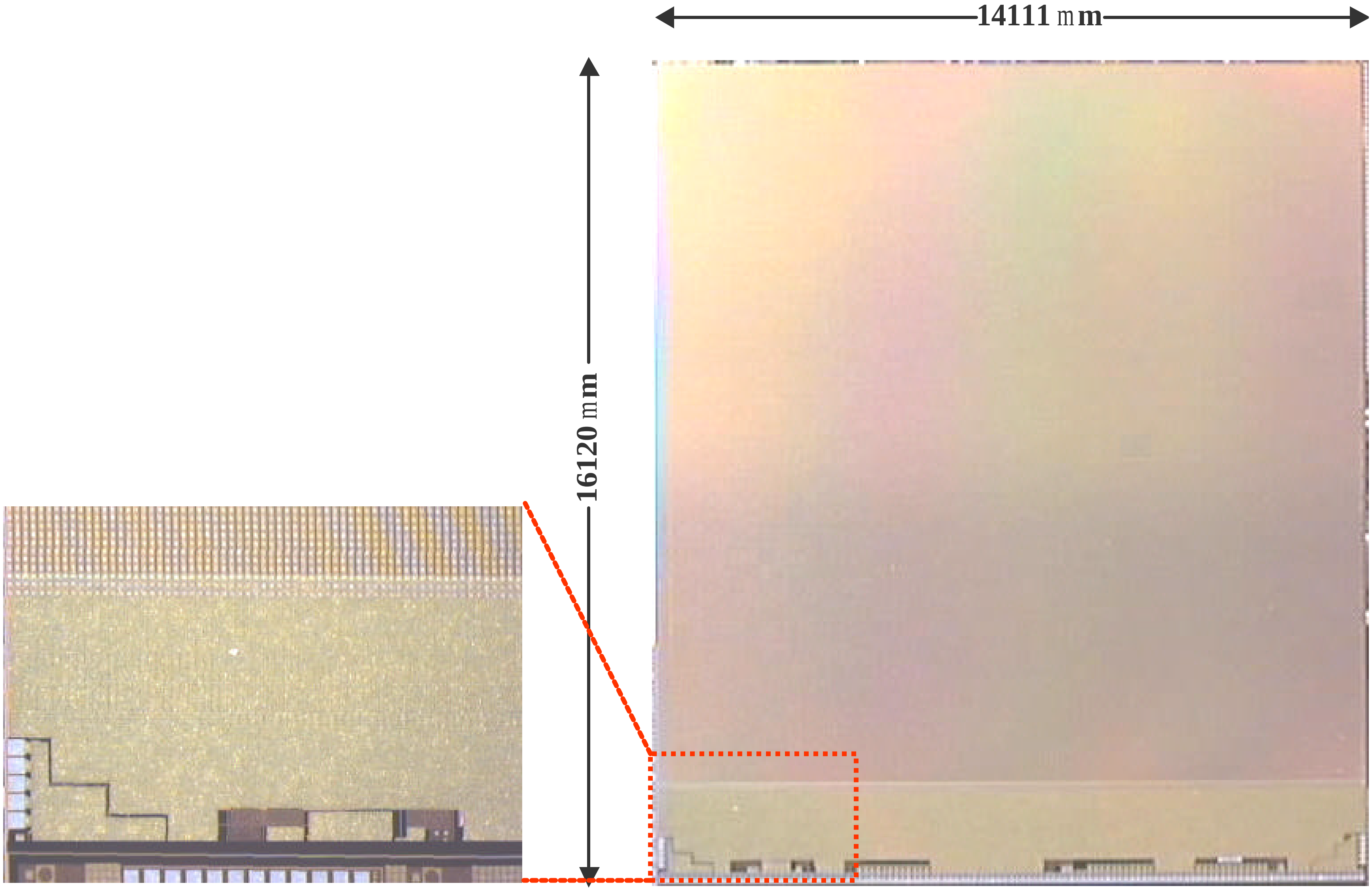
Medipix2 Pixel Cell Layout



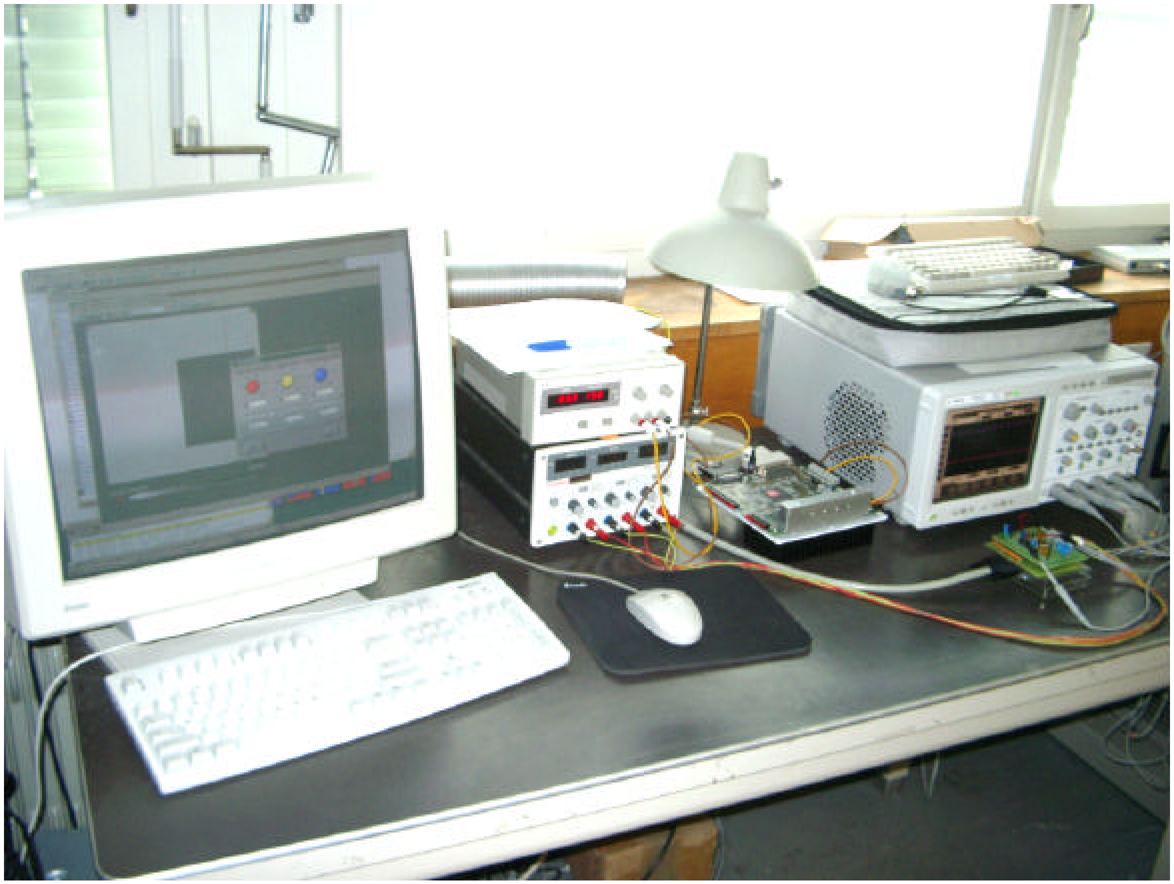
Medipix2 Chip Architecture (I)

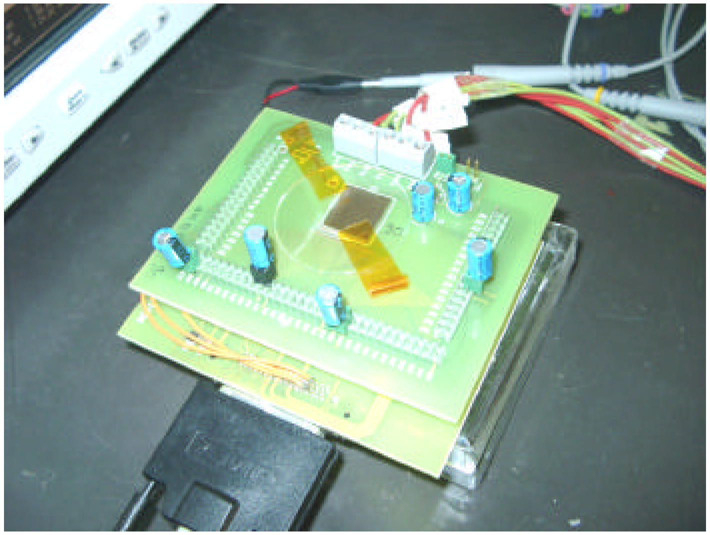


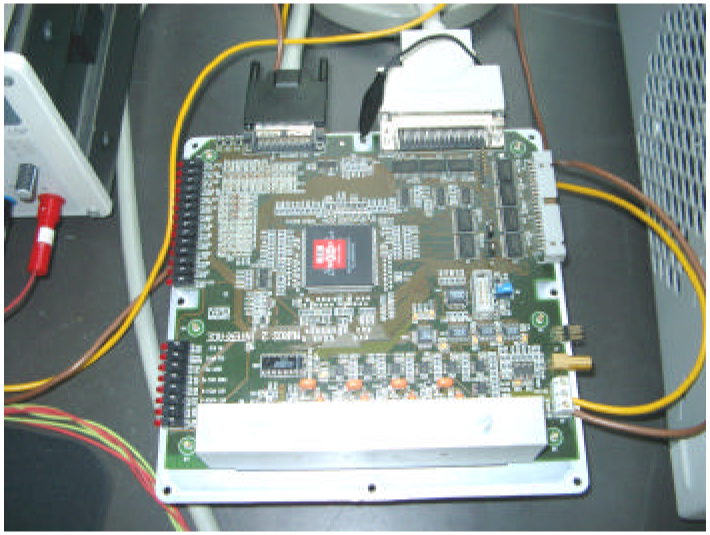
Medipix2 Chip Architecture (II)



Measurement Setup

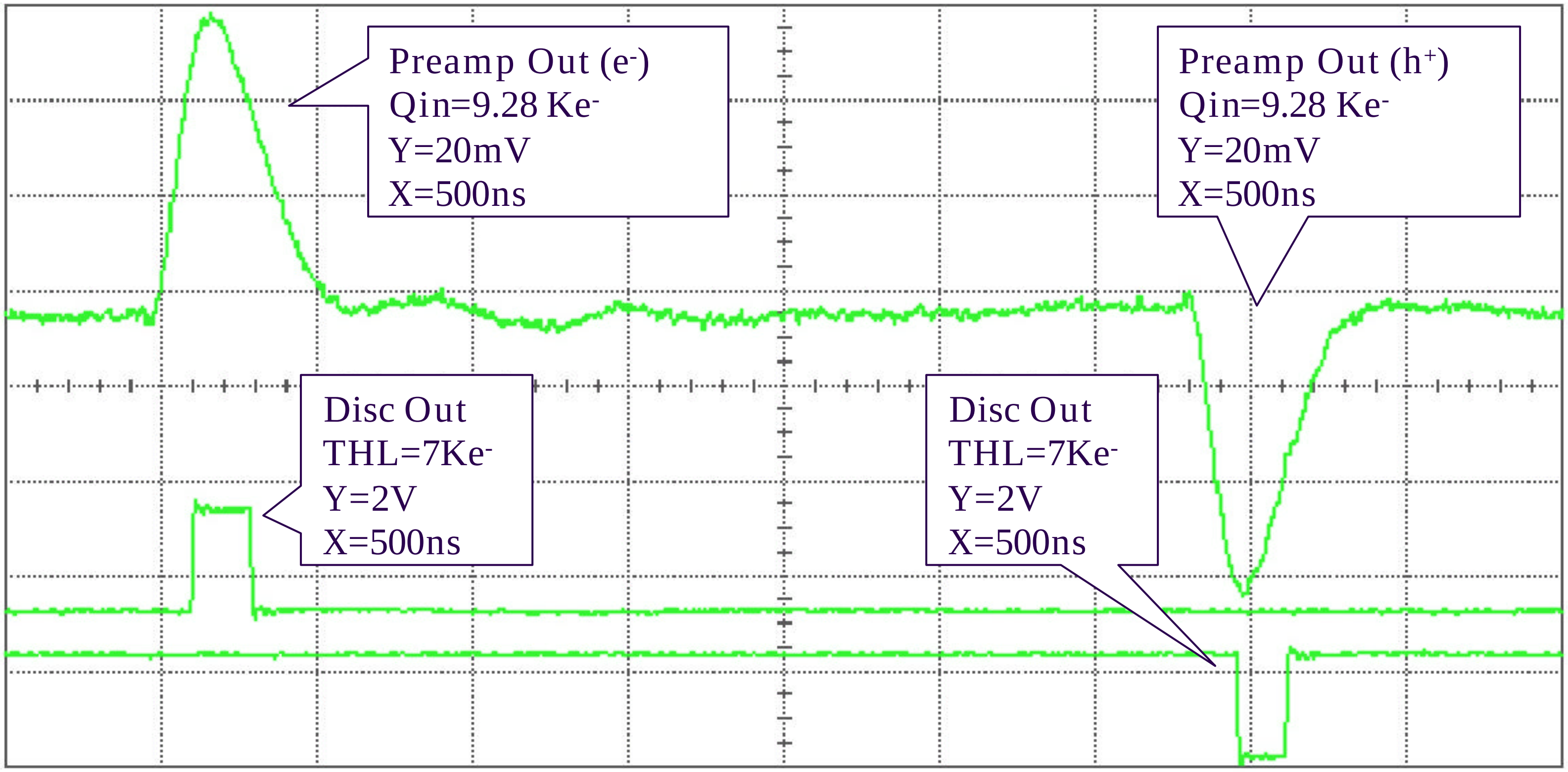






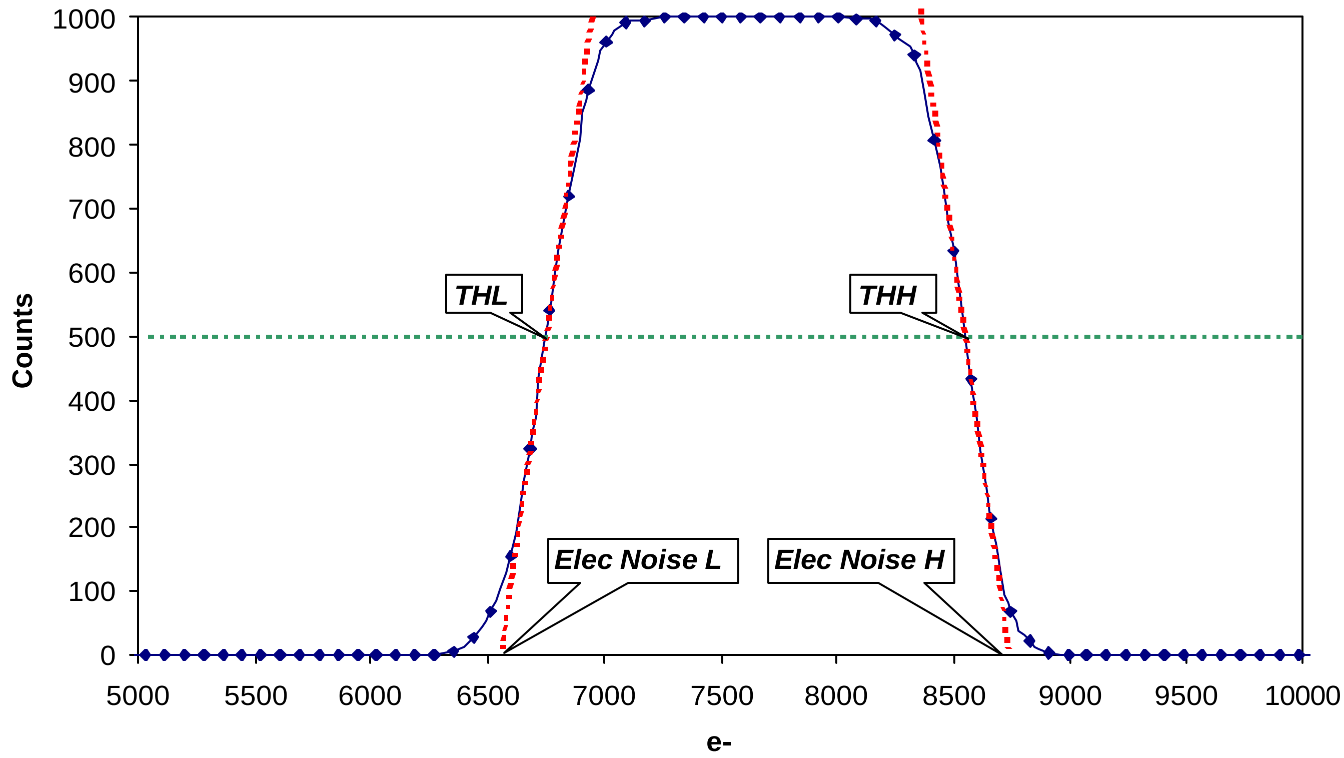
Preamplifier and discriminator measurement

- Measurements have been done using the Test output Pads and applying a voltage test pulse to the on-pixel injection capacitance.

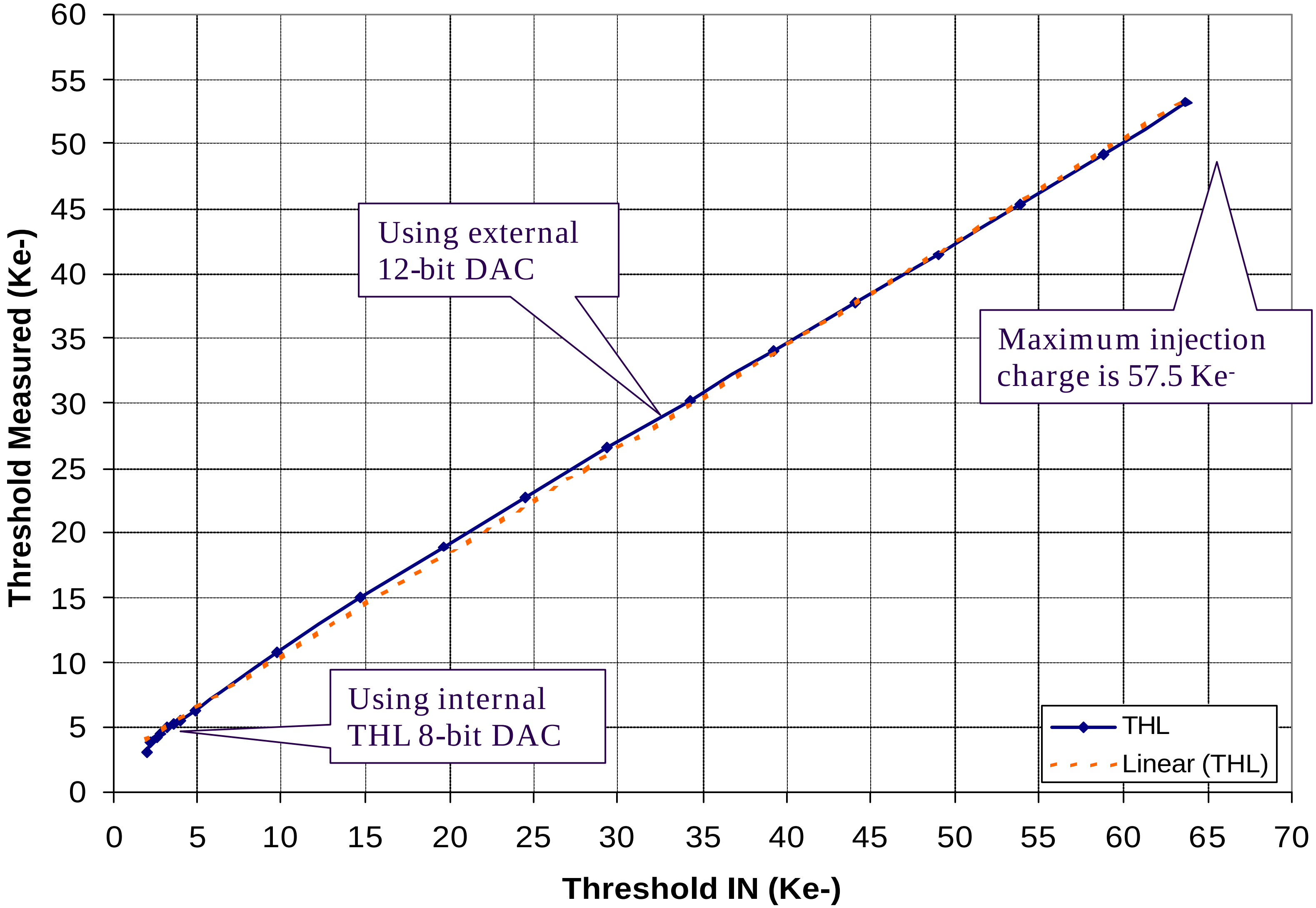


Measurements and Calibration

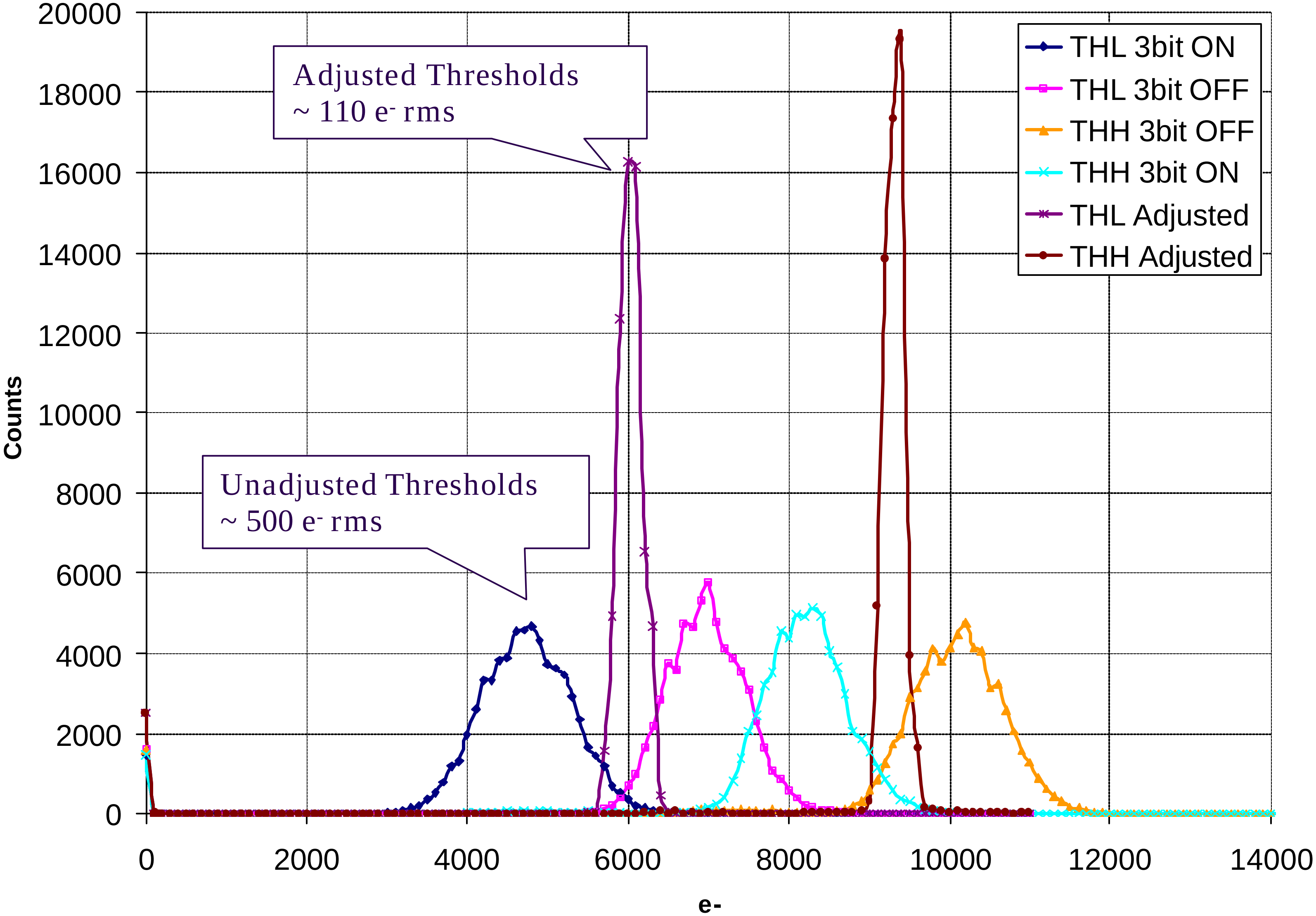
- All the reported measurements are done using the electronic calibration (Injection capacitor + external voltage pulse).
- The 8fF injection capacitor nominal value has a tolerance of 10%.
- The dedicated Muros2 readout system (Muros2 + Medisoft) has been used



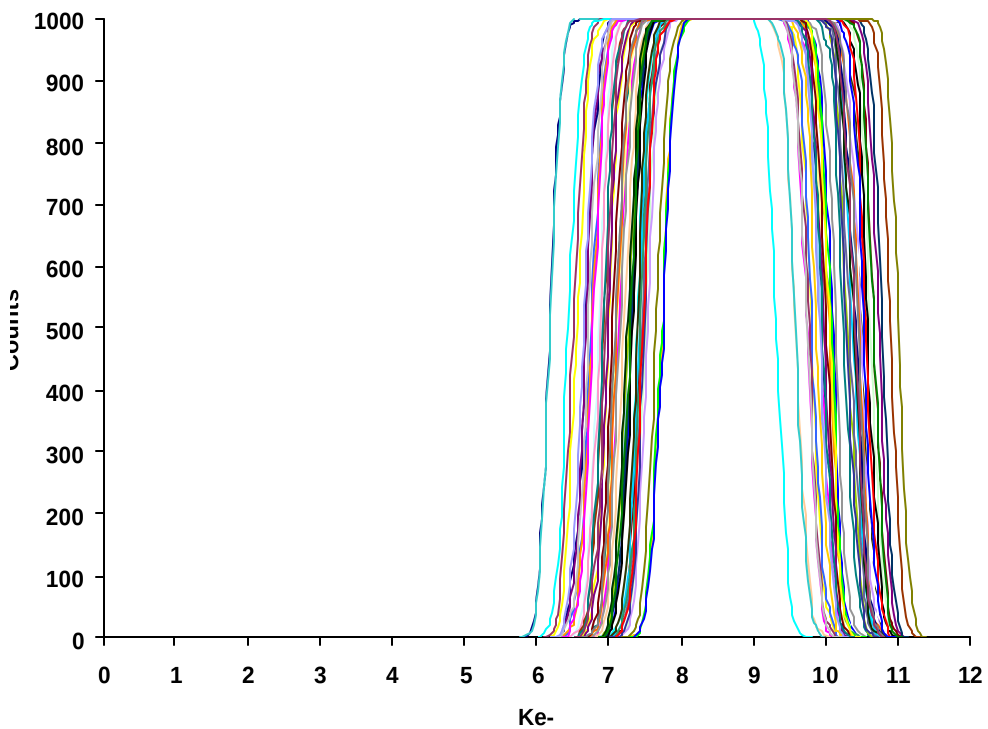
Threshold Linearity



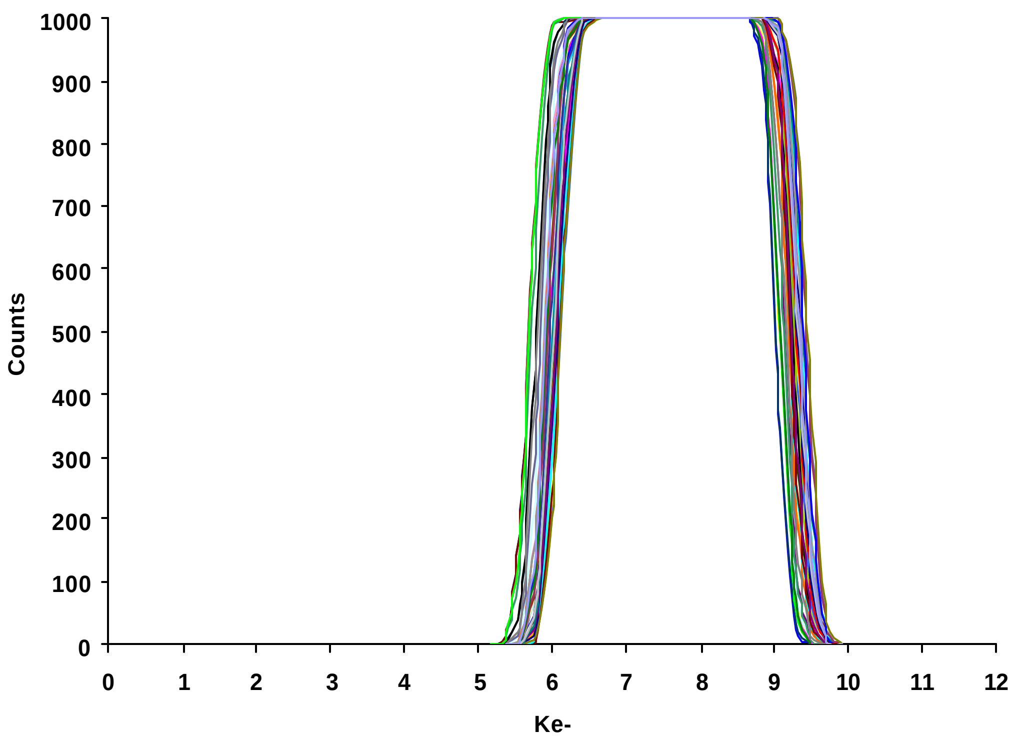
Threshold Equalization (I)



Threshold Equalization (II)

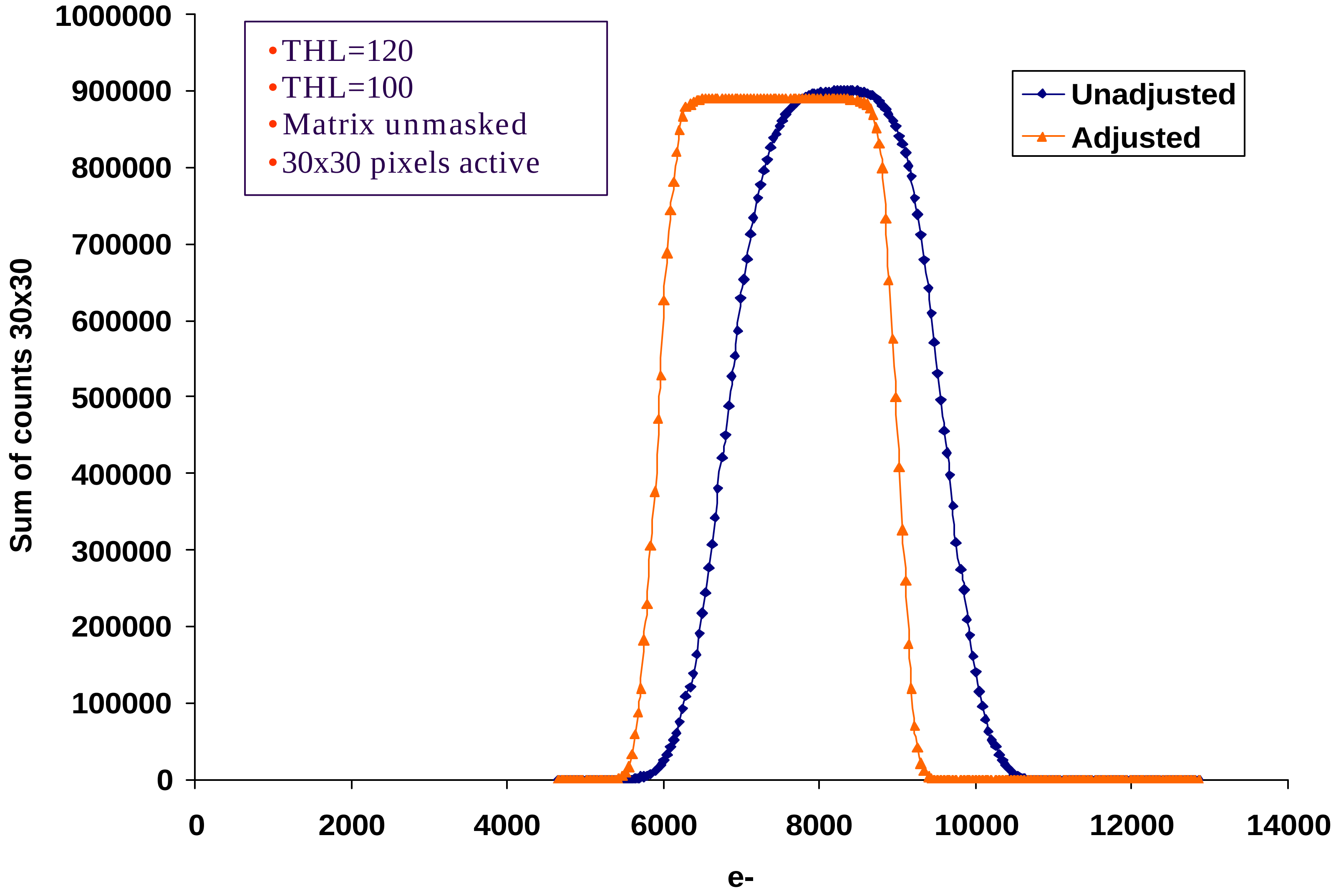


1 row of **Unadjusted** pixels

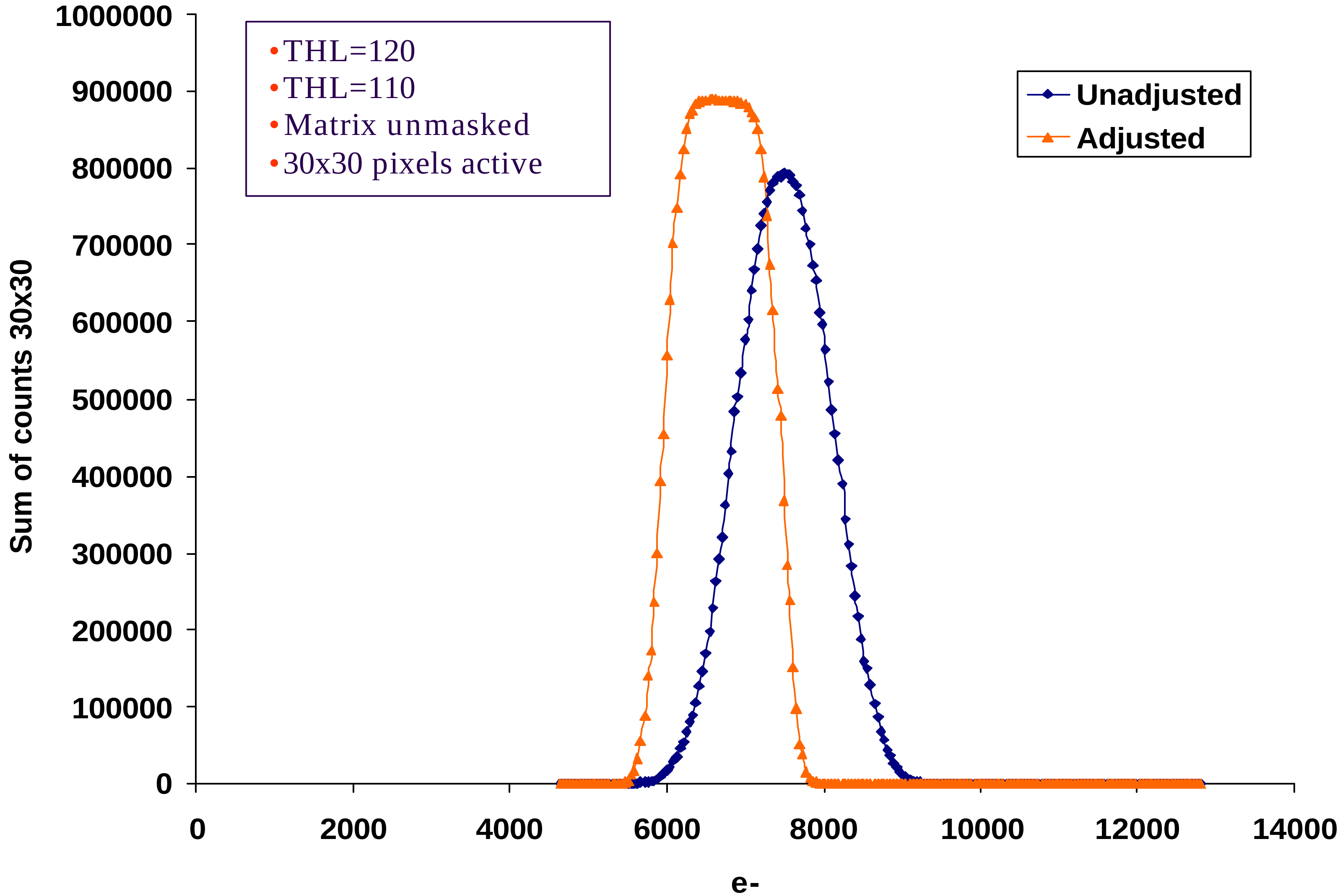


1 row of **Adjusted** pixels

Threshold Equalization (III)

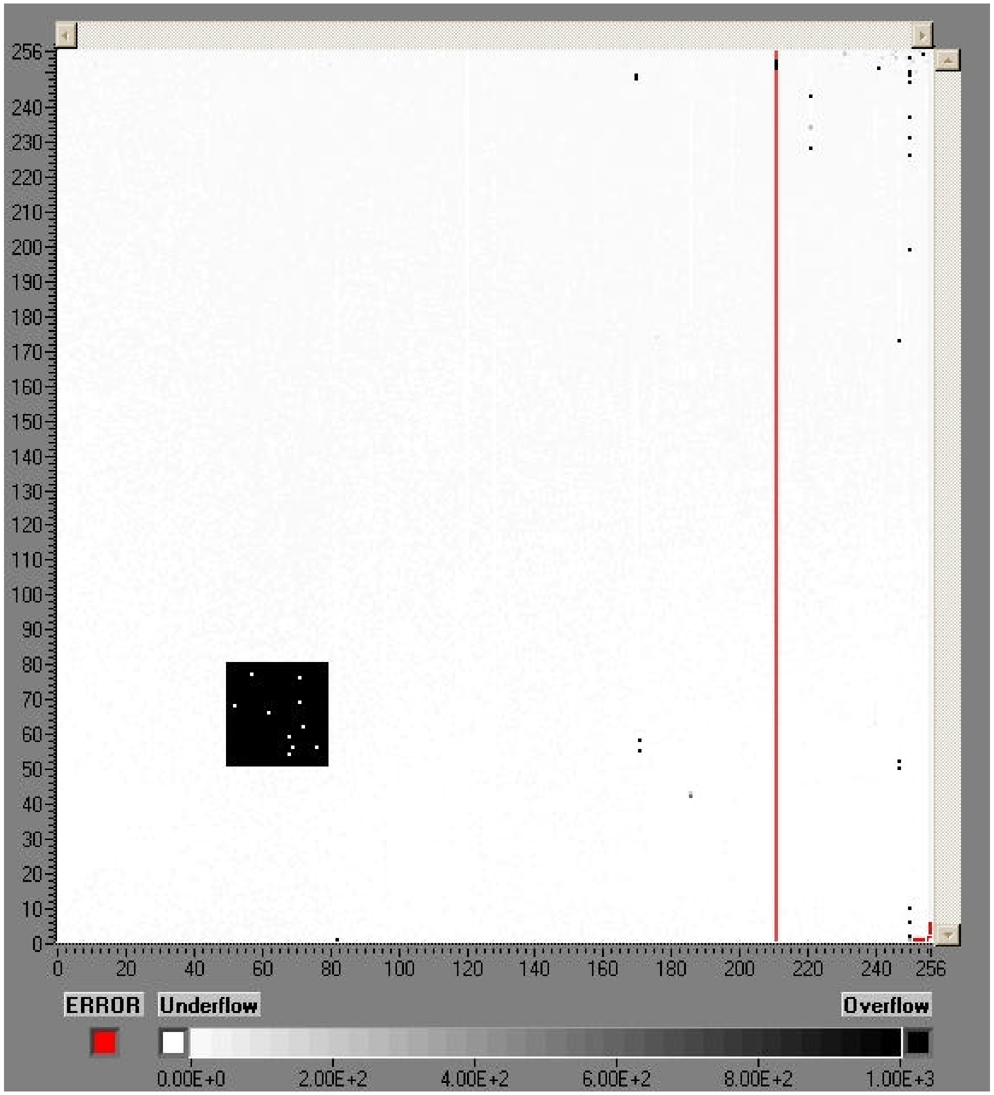


Threshold Equalization (IV)



Threshold Equalization (V)

- THL=140 (2.8 Ke⁻)
- Injection of 1000 pulses of 3.6 Ke⁻
- Matrix unmasked
- 30x30 pixels active



Summary of the Electrical Measurements

	Electron Collection	Holes Collection
Gain	*12.5 mV/ke$^-$*	*13.25 mV/ke$^-$*
Non linearity	*<3% to 100 ke$^-$*	*<3% to 80 ke$^-$*
Peaking time	*<200 ns*	
Return to baseline	*<1ms for Qin <50 ke$^-$*	
Electronic Noise	*S nL~ 105 e$^-$ S nH~ 105 e$^-$*	
Threshold dispersion	*S nTHL~ 500 e$^-$ S nTHH~ 500 e$^-$*	
Adjusted Threshold dispersion	*S nTHL~ 110 e$^-$ S nTHH~ 110 e$^-$*	
Analog power dissipation	*~8 mW/channel for a 2.2 V supply*	

Periphery Measurements

- The 13 DACs perform as simulations
- Fast shift register works at > 100 Mhz*
- Peripheral logic works to > 100 Mhz*
- Serial/parallel I/O work
- LVDS drivers and receivers work to > 100 MHz*

Radiation Tolerance Measurements

- 10 keV X-ray source
- Chip under bias conditions
- Applied dose rates:
  - 3.9 krad/min up to 150 krad
  - 8.04 krad/min from 150 krad to 500 krad
- Analog power supply current increase from 200mA to 260 mA
- Digital power supply current increase sharply @ 200 krad reaching 1100 mA @ 500 krad
- After 1 week of annealing at 100°C the power supplies current recovered to pre-irradiation values
- Chip showed normal behavior untill 200 krad and still functioning after annealing at 500 krad

Conclusions

- A prototype chip consisting of 256x256 pixels has been produced with a square pixel size of 55 µm. Each pixel has around 500 transistors.
- Using the dedicated Medipix2 readout system (Muros2 and Medisoft4) complete electronic measurements and threshold calibration have been done.
- Adjusted threshold variation ~110 e^- rms for both levels of discrimination.
- Electronic Noise ~105 e^- rms.
- Difficulties to lower the threshold under 2.5 Ke^- with the present setup.
- The chip is radiation tolerant until at least 200 Krad.

On-going work

- A new chipboard card is ready to be tested with improved decoupling and power distribution.
- Probe tested wafers have been sent for bump bonding to high resistivity standard p^+ on n silicon detectors.
- This should allow an absolute calibration with radioactive sources.
- Other materials will be tried later (CdTe, GaAs, etc…)

Future Prospects

- **With pixel shrinking charge sharing starts to dominate the detector behavior.**
- **Hexagonal pixels (on the detector side) become attractive.**
- **New front-end electronics architectures are needed.**
- **Some ideas are presented in a recently accepted paper for publication in the NSS/MIC IEEE journal.**
- **Using deeper sub-micron CMOS a whole spectrum of new possibilities opens with e.g. time-resolved measurements, very high dynamic range applications, colour X-ray imaging…**