Development of 3-D Packaging for High-Bandwidth Massively Paralleled Imager

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Overview

- Proton Radiography and Detector Requirements
- Signal Processing Electronics
- Hybrid Approach
- High-Density Interconnect (GE - HDI)
- Stacking Process Flow
- Illustrative Examples
- Balance Sheet and Future Work

Proton Transmission Radiography

- **Probing particles: high-energy protons**
- **Proton flux attenuation:**
  - **nuclear collisions**
  - **multiple Coulomb scattering**
- **Magnetic lens forms an Image of the Object**
- **Multiple short beam pulses**
  - **multiple views of dynamical object evolving in time**
  - **or static radiographs**

Magnetic Lens for pRAD

Object plane

Image plane

7.94 m

Horizontal plane

Diffuser

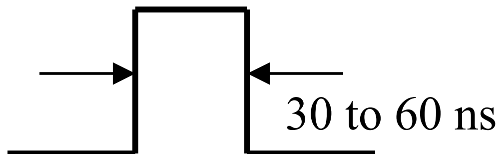
10.49 m

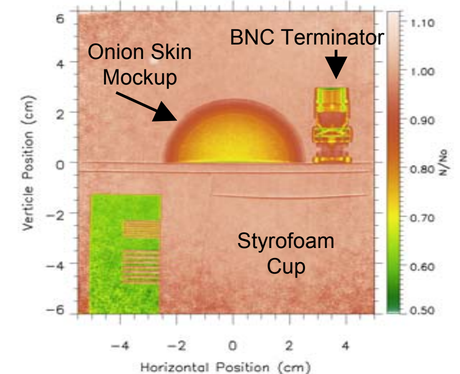
Collimator

Vertical plane

-I

Proton pulses with variable pulse length and pattern are possible

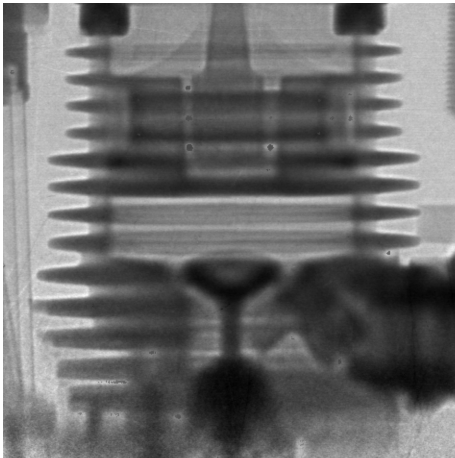




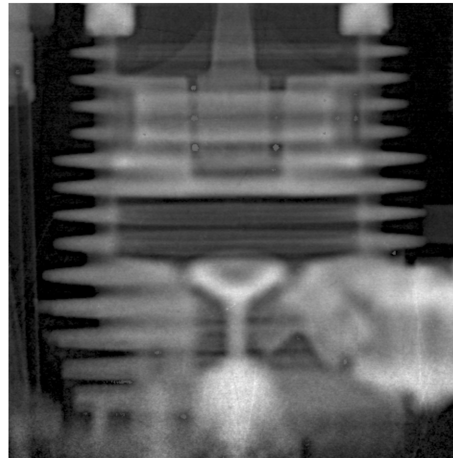
Proton Radiography - Abel inversion

(tomography assuming axi-symmetry)

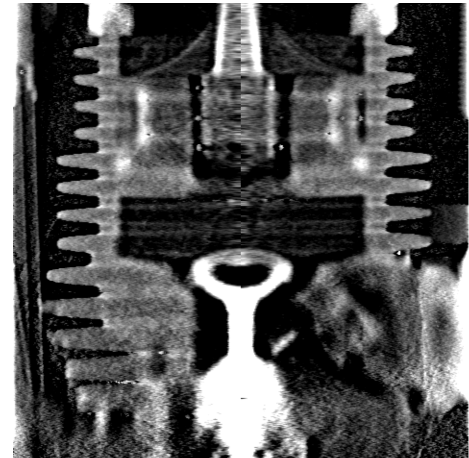
Radiograph



Areal density



Volume density



Fast Imager for pRAD Requirements

- Number of frames: 32 (128 preferable)
- FOV: 12×12 cm^2
- Array Size: 1024×1024 pixels
- Inter-frame time: 180/ 358 ns
- Pulse duration: 30 – 50 ns
- Dynamic Range: 11 to 12 bits
- “Well depth” (saturation charge): 2×10^6 e^-

- 100% Fill Factor and QE > 80%

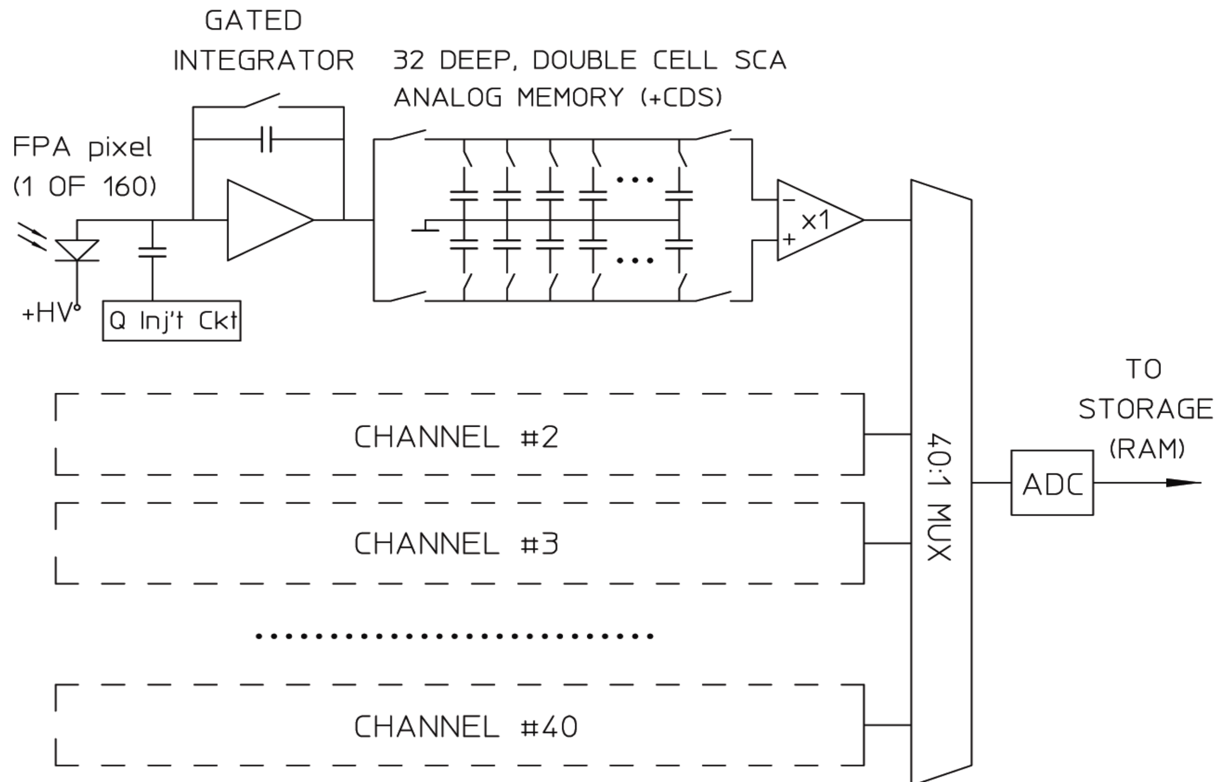
Hybrid Approach

Hybrid imaging technology allows:

1. 100% fill factor
2. Optimize sensor & electronics independently
3. Thermal mismatch minimal
4. Same electronics with different type sensors

- **Flip-chip bump bonding, to interconnect two layer (complexity, cost, risks)**

Front-End and Readout Electronics



Channel electronics require area far exceeding pixel size

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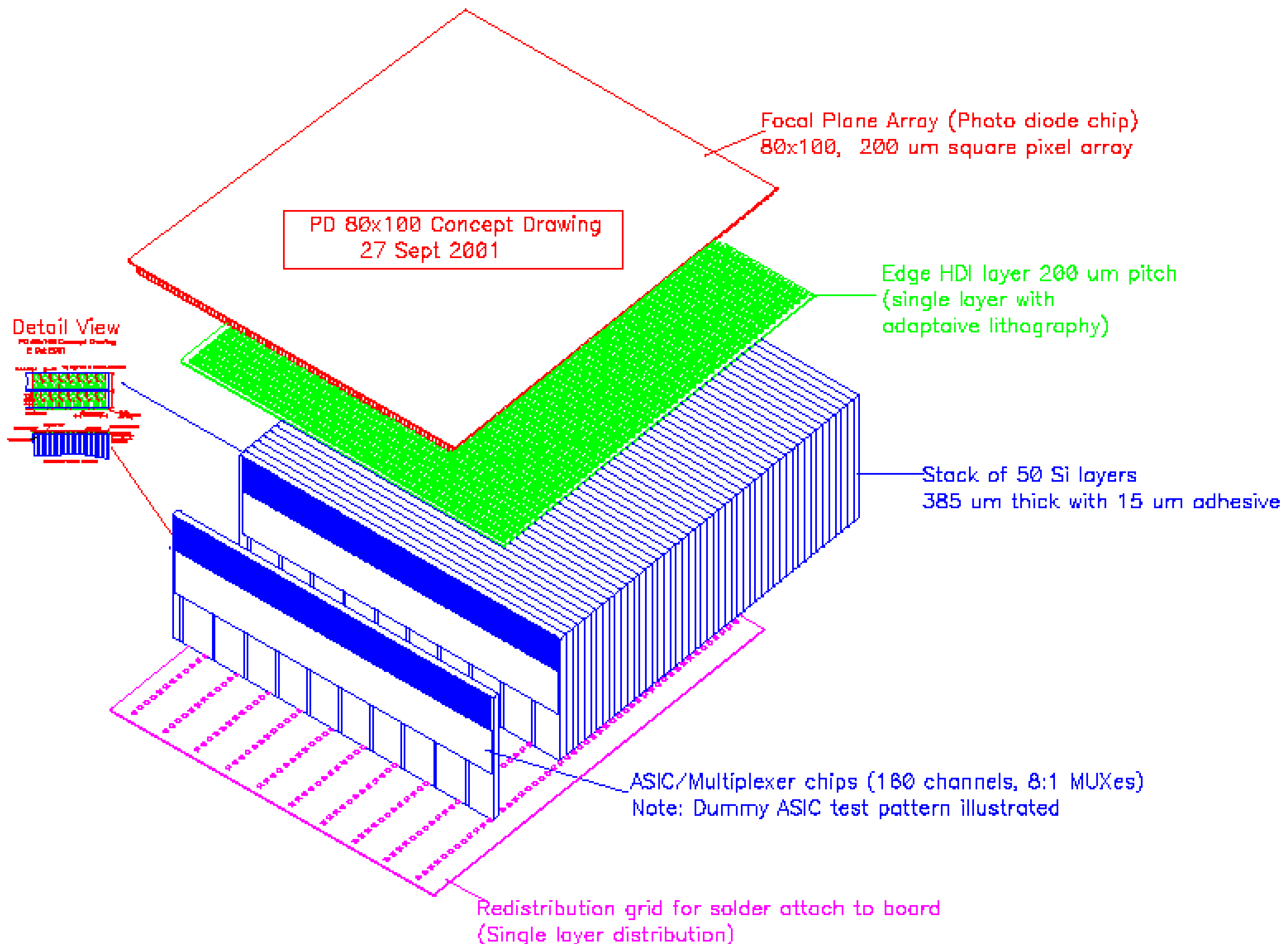


Emulation IC Slice with 16:1 MUX and Integral Heater Assembly

17.052

4.727

.500

10.400

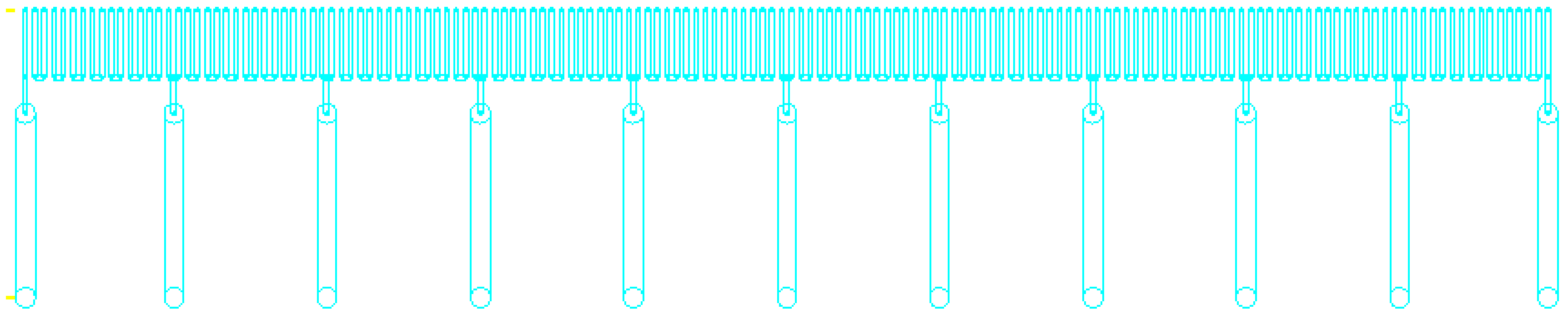
.150

Heater & Contacts

~ 4.5 ohms @ 3.3Vdc = 2.42 Watts / Slice x 50 = 121 W

~ 4.5 ohms @ 1Vdc = 0.2222 Watts / Slice x 50 = 11.11 W

16:1 Series Path Created in the Test Design & Arrayed in 50 Series Links



3D Stacking - Process Flow: *Step I*

Chip - Scale Package ("Slice") Fabrication

1) Attach thinned Si die to Kapton using GE Chip-on-Flex Process

2) Encapsulate Die in Plaskon molding material

3) Laser Drill vias to die bond pads

4) Metalize and pattern interconnect to bring out connections from die

5) Apply adhesive layer to top surface (Kapton/interconnect)

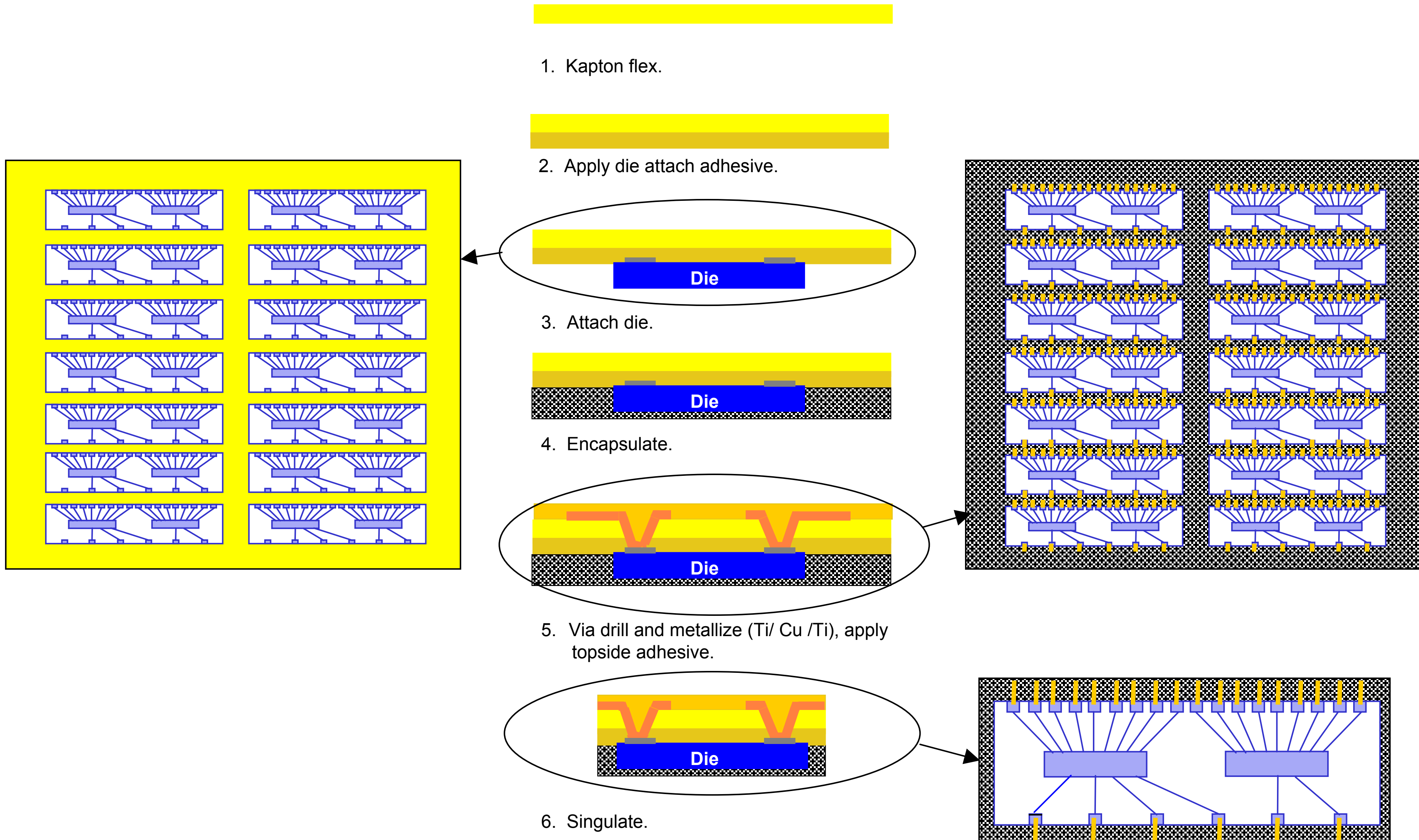
6) Grind Slice backside (Plaskon) to desired thickness (~400μm)

7) Singulate individual die from Plaskon molding

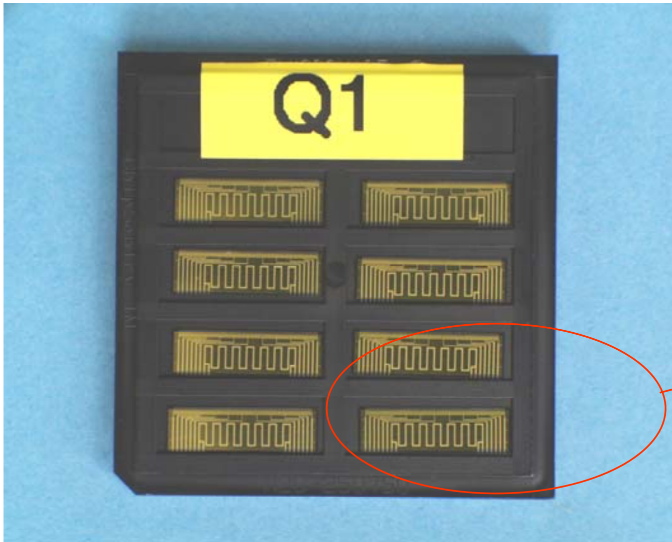
-These are now the "slices" that will be stacked together

2D Chip Scale Slice Framing Process

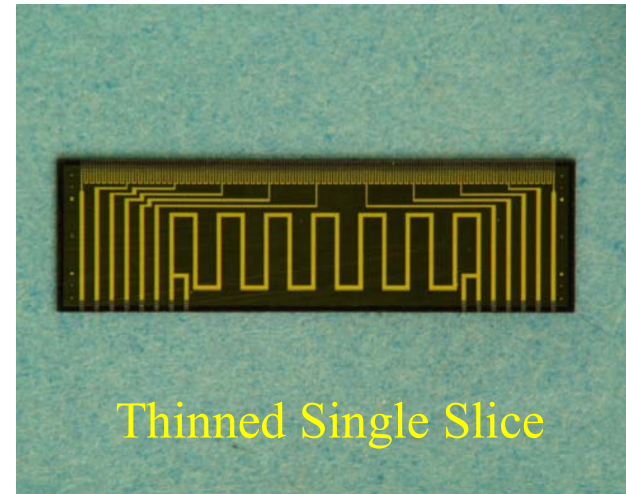
GE Chip-on-Flex Process:

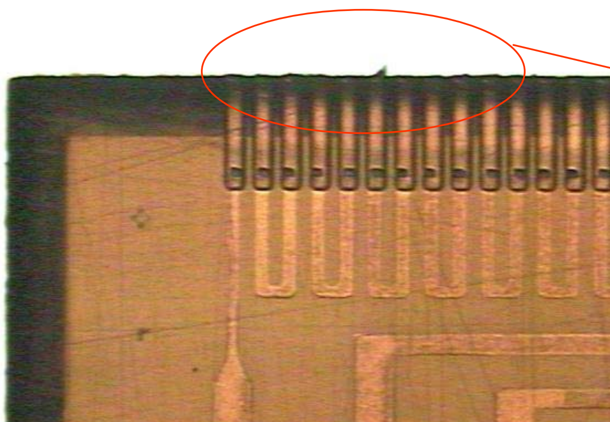


Slice Processing for 3D Stack - Step I

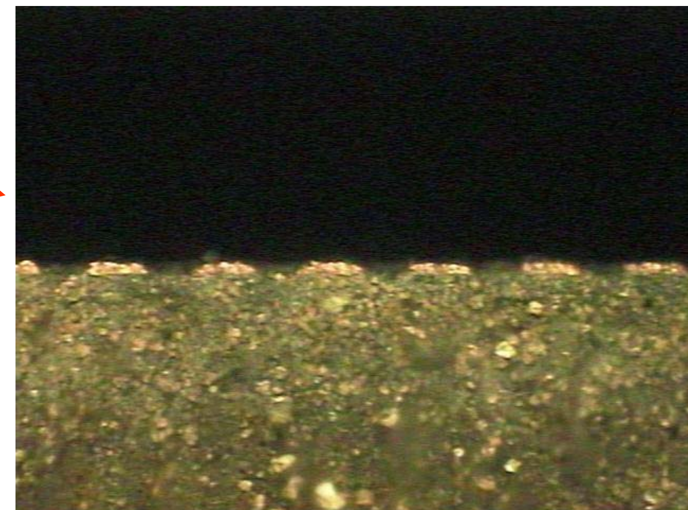


Individual slices in waffle pack





Cut out slice w/ 200µm plaskon boarder



X-sectional view of fingers

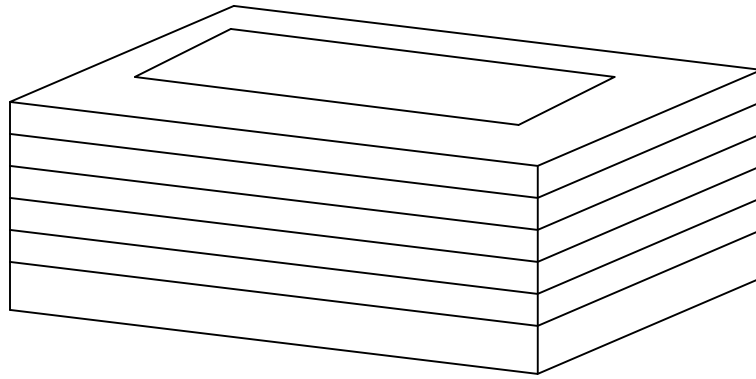
3D Stacking - Process Flow: *Step II*

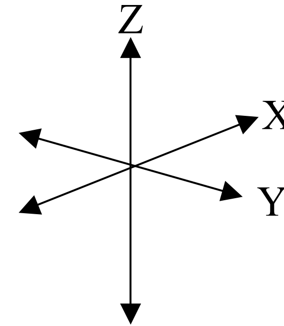
Assembly of 50-Slice Stack

1) Clean "slices" in ultrasonic bath
2) Measure thickness of each "slice" and stack accordingly to minimize run-out
3) Stack 50 "slices" in stacking fixture/ jig and cure in oven
4) Remove assembled stack from jig and grind edges (~25µm) to expose HDI traces/ connections to encapsulated die

- Stack is ready for lamination of top and bottom (interposer) interconnect layers

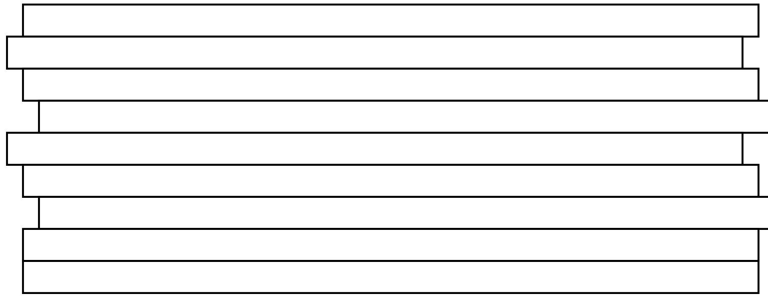
CSP Stacking Runout & Tolerance Issues

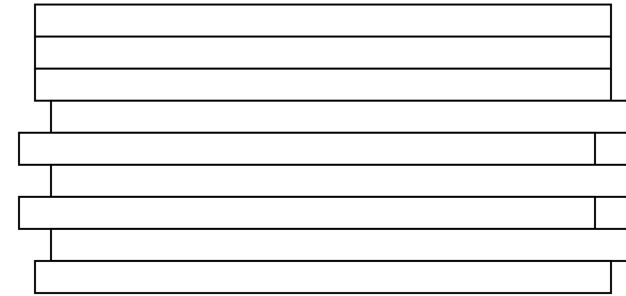




Possible
Run out In all Axis !!

Θ Rotational issues for
Each of 50 pieces not shown

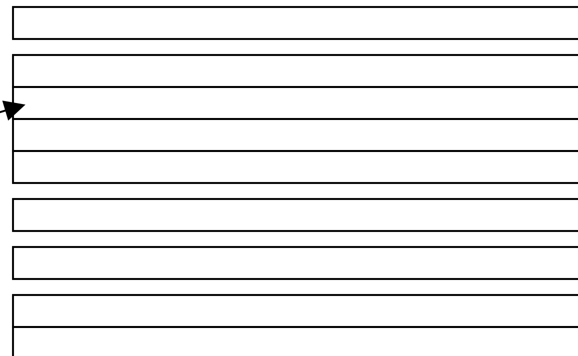




Y
Variation
ESI and stacking

X
Variation
ESI and stacking

Chip Scale Packages (CSP)



Z
Variation
Glue and grinding

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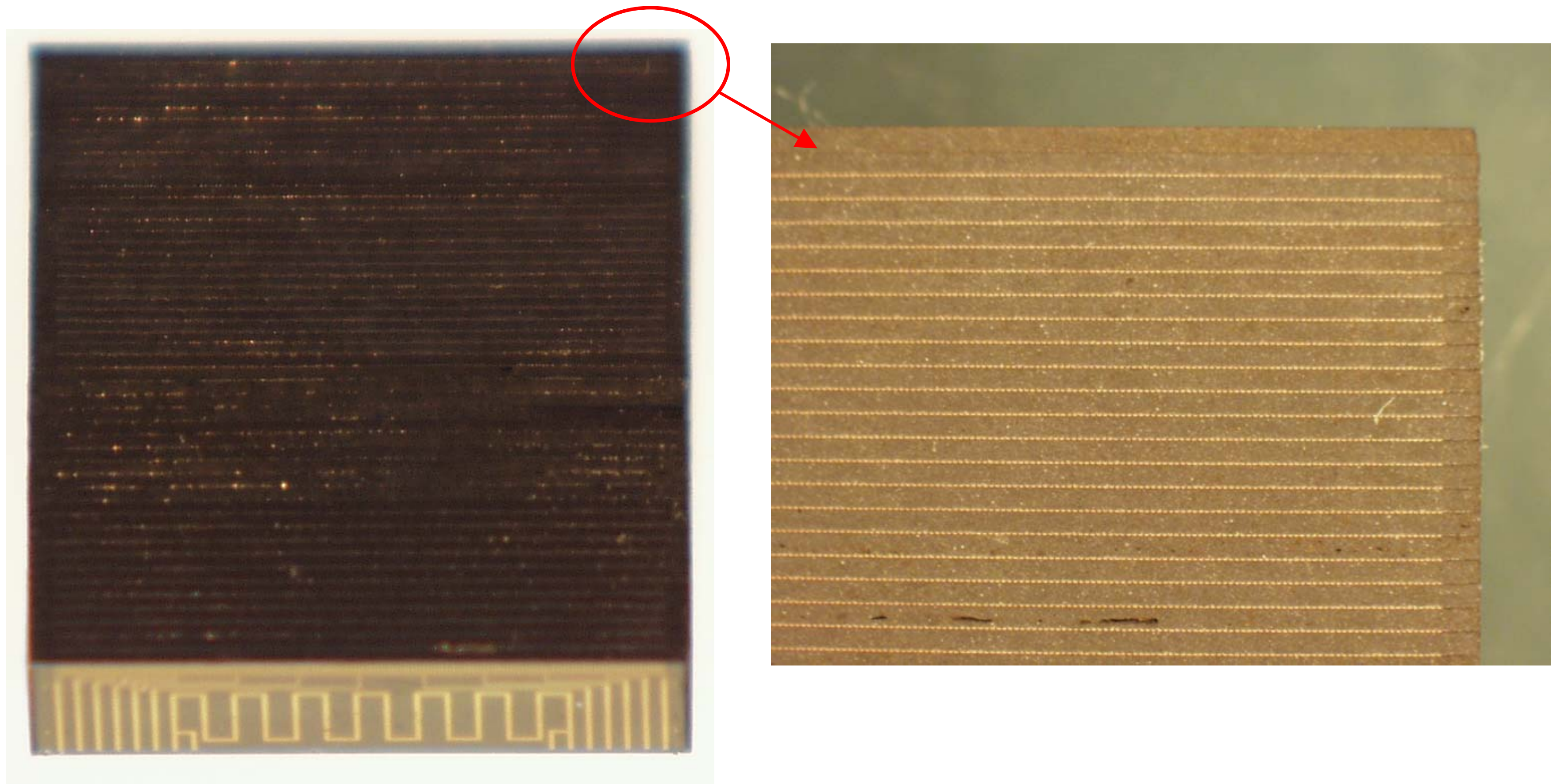
“Cube” Assembly Jig

Assembled Cube - Top View
Top and Bottom Surfaces Ground



3D Stacking -Process Flow: Step III

Top (8000 I/O) and Bottom (750 I/O) Interconnect Layer Fabrication

1) Laminate kapton to top side of stack in processing carrier
2) Laser Drill vias to exposed HDI connections on side of stack
3) Metalize and pattern interconnect (This is an **adaptive pattern** that **conforms** to the **actual geometry** of the **stack**)
4) Laminate 2nd layer of kapton
5) Laser Drill vias to 1st layer of HDI pattern
6) Metalize and pattern interconnect (This pattern will form the 8000 I/O grid)
7) Apply Soldermask layer to isolate 8000 I/O
8) Remove stack from processing carrier to access 750 I/O side
9) Repeat process for the 750 I/O side (bottom) of stack in processing carrier
10) Verify planarity (< 5µm)

- Stack is ready to be bump bonded to the sensor and PCB back-end electronics layer

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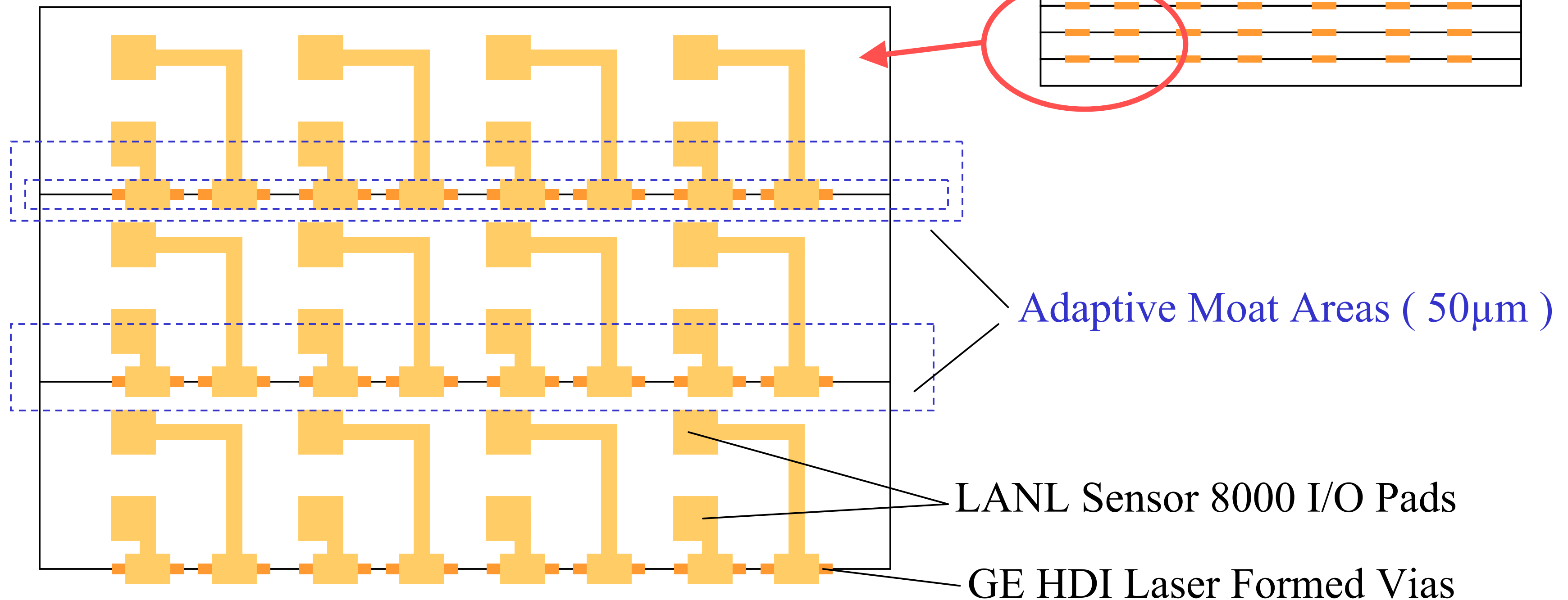
3-D Stack Adaptive Run-out Issues

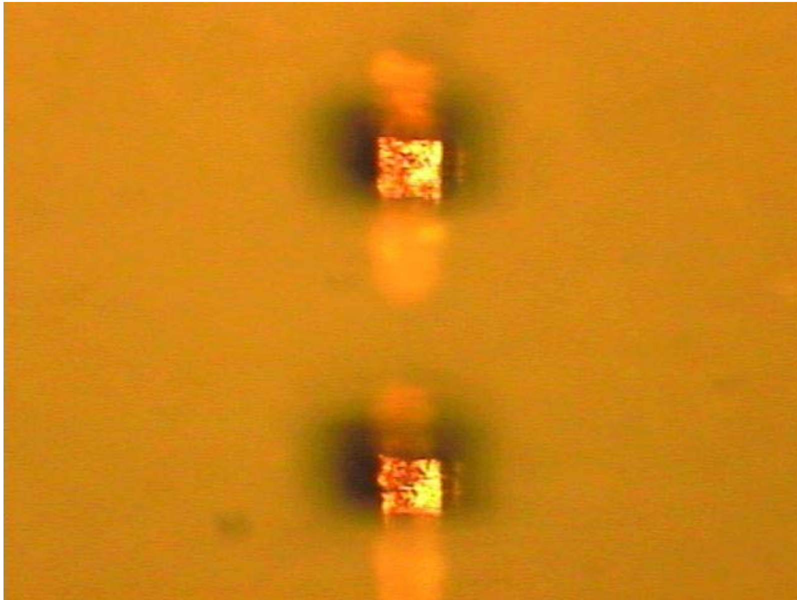
Slice Packets Are Used To Control Pad Tolerance Runout (max. 50µm Window)
Packets May Be Varied In Thickness For Tolerance Back To Grid

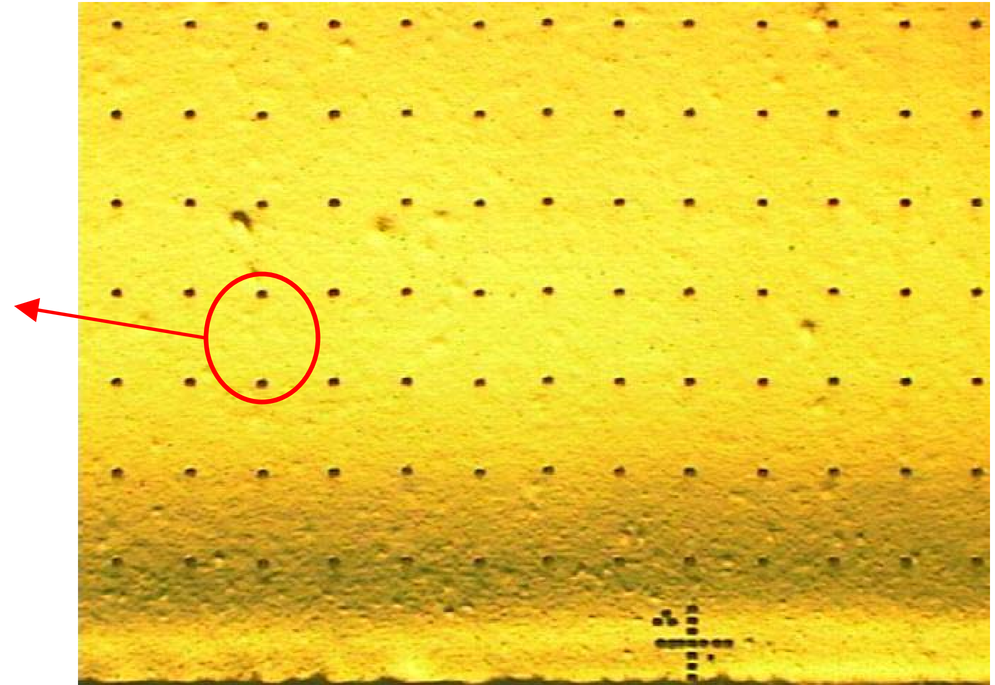
Adaptive Lithography Laser Region

Adaptation of entities in inner box can only adapt as far as the boundary of the outer box!



Laser Drilled Vias

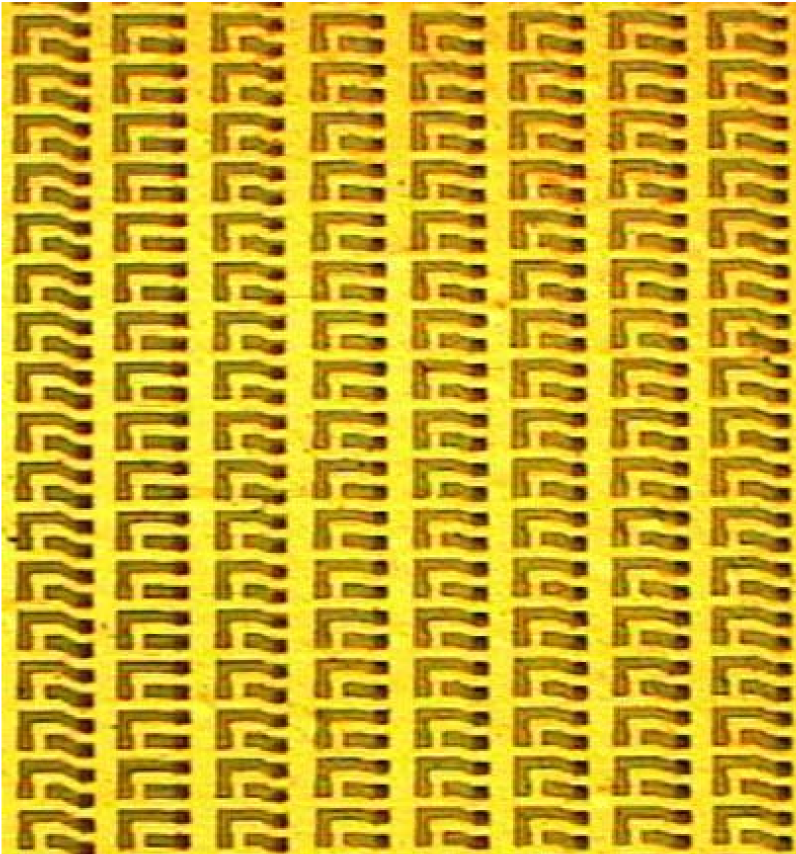


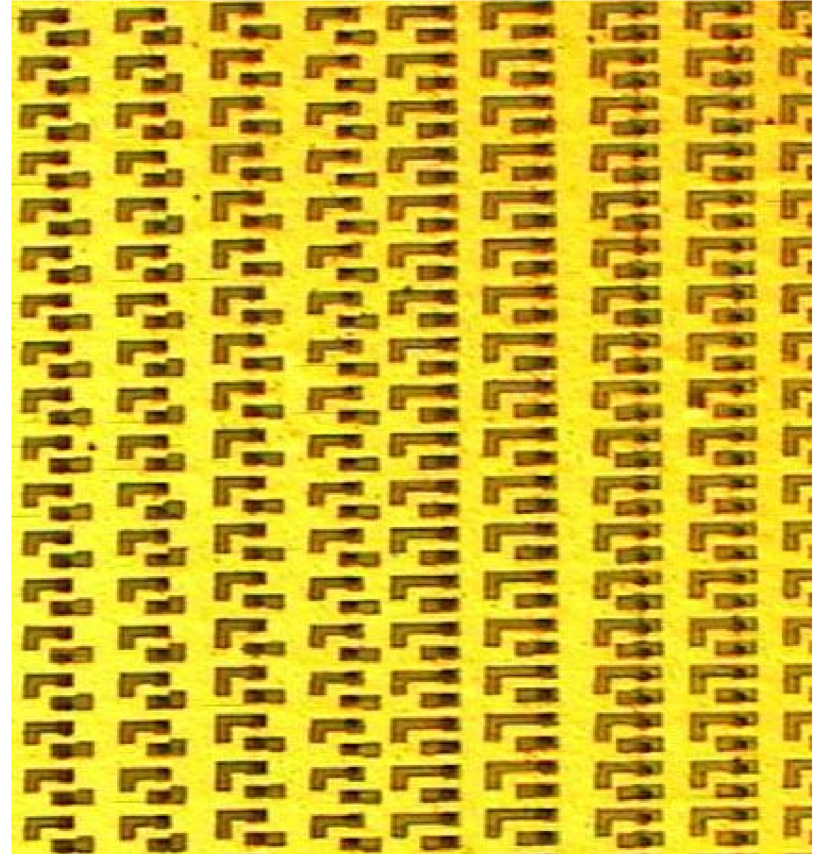


Bottom side, 750 I/O drilled Vias

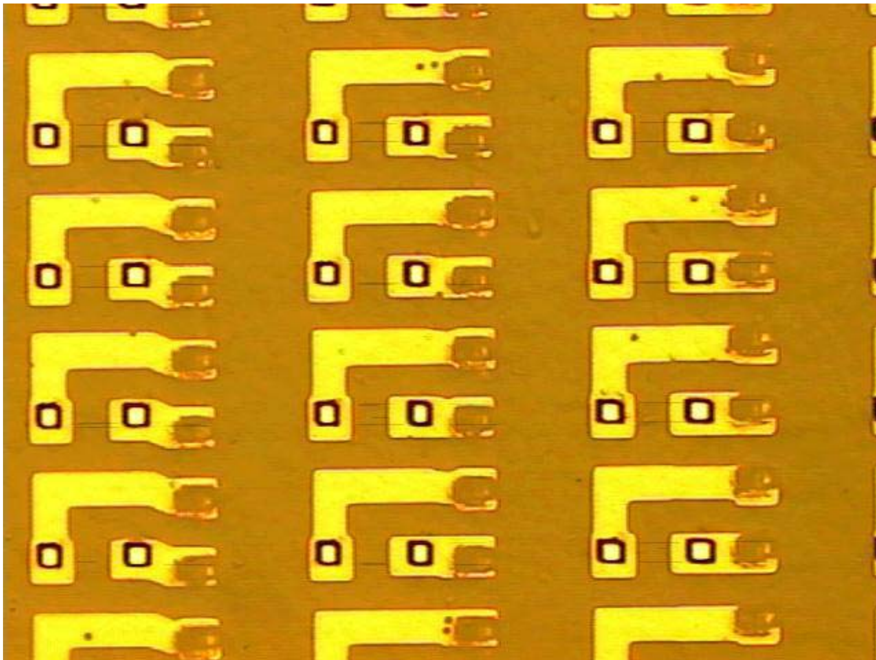
Top (8000 I/O) HDL Layer -1: MT1

Adaptive Lithography at Work

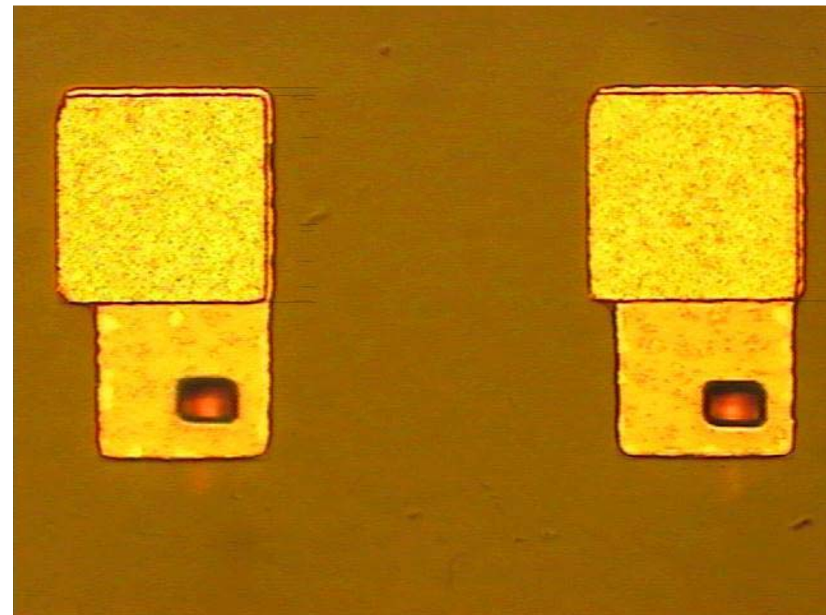




Top HDI Interconnect and Bump Pads
Layer-2: MT2

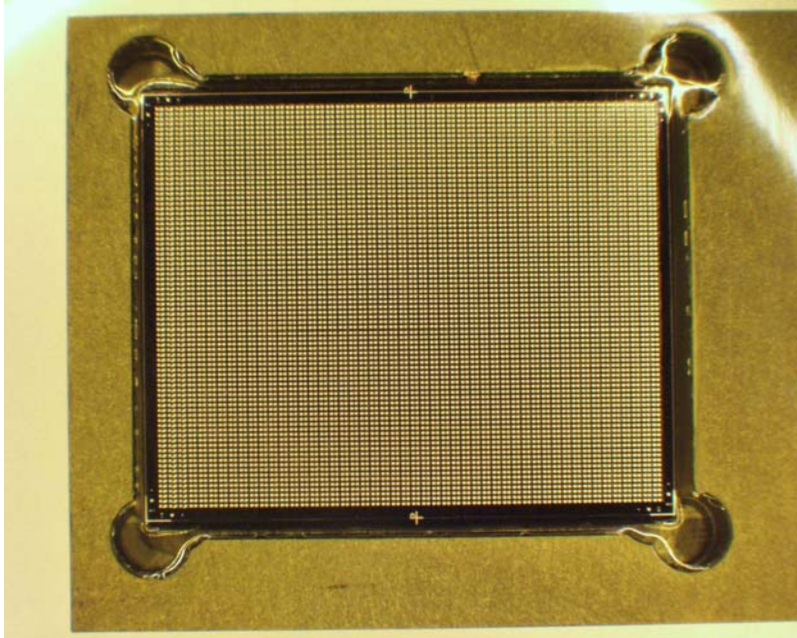


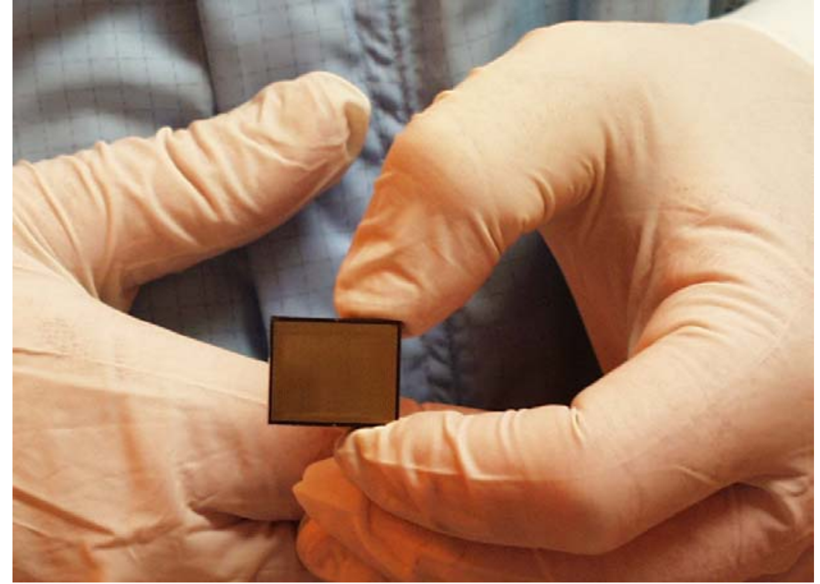
Top (layer-2) kapton lamination
showing vias to layer-1
before deposition of Bump Pads



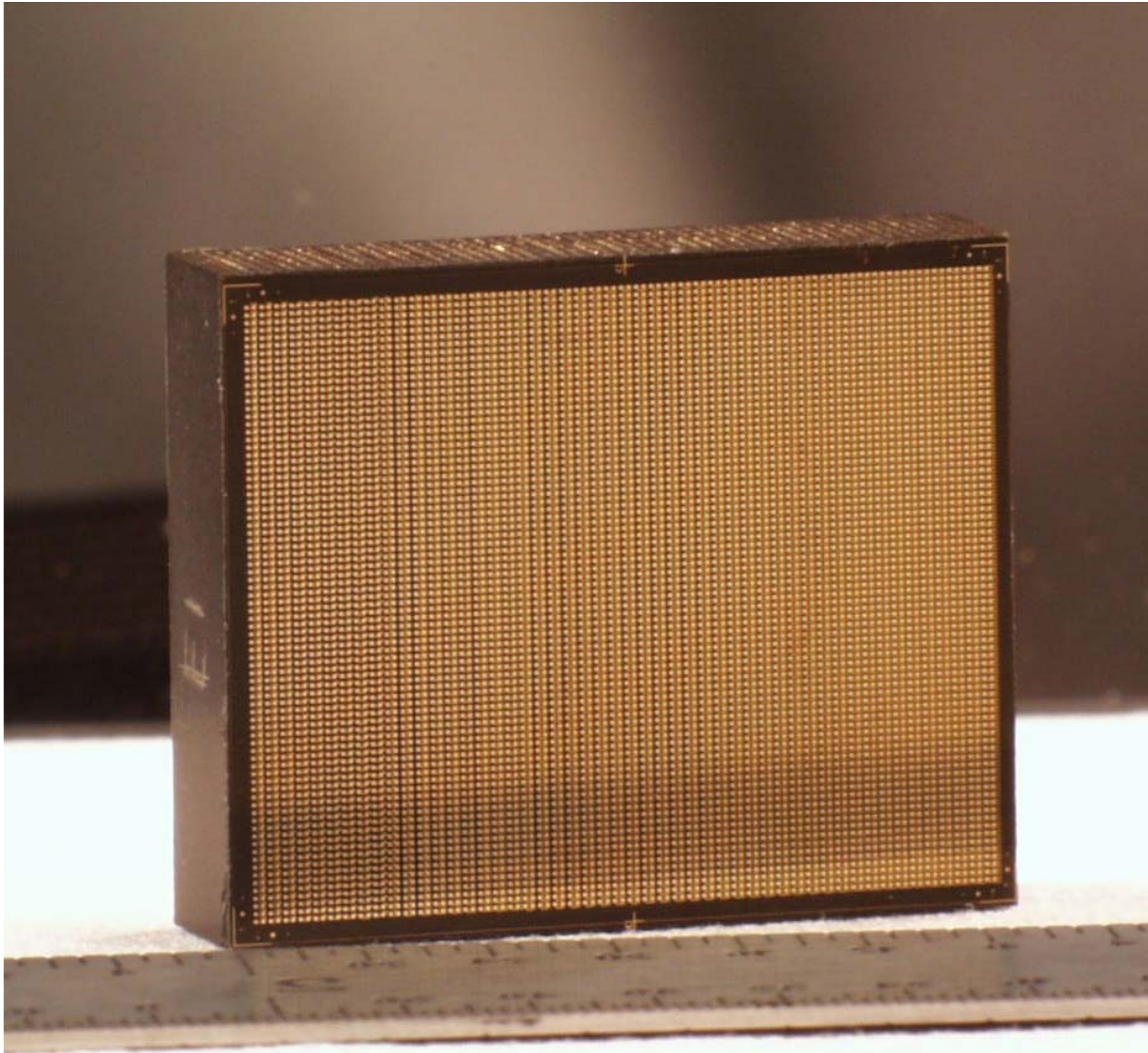
Vias and Finished Bump Pads

Cube with Laminated HDI Layer





Cube – Close-Up



3D Stacking - Process Flow: Step IV

Final Assembly/ Hybridization of Photo-Sensor to Stack and Stack to Base PCB

1) Done at outside vendor (PFCC)
2) Apply polymer bumps to photo-sensor via stencil mask (8000 pads)
3) Apply polymer bumps to 8000 I/O side of stack
4) Align and assemble sensor and cube
5) Cure polymer bumps (**overnight at <u>room temperature</u>**)
6) Repeat process for bottom layer

   (to PCB with back-end electronics; 750 I/O on 0.4mm grid)

- Stack ready for testing (µP-controlled: continuity verification, electrical shorts test, power dissipation)

3-D Slice-Stack Assembly

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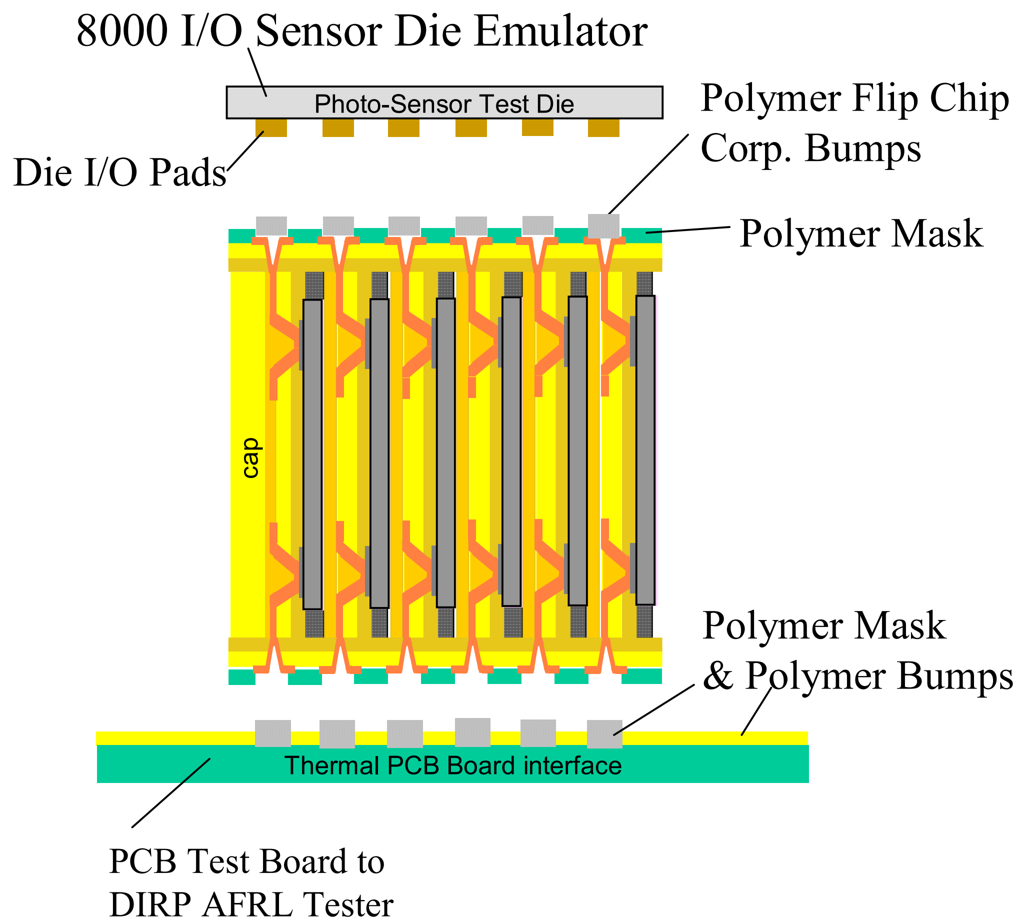
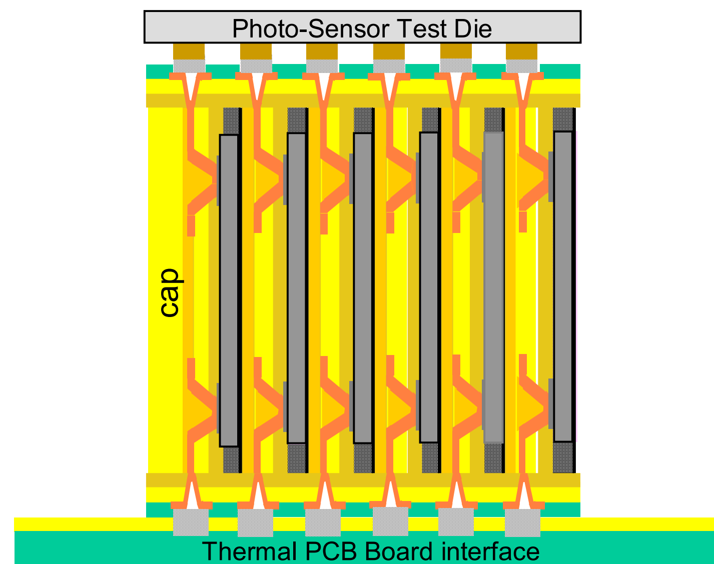
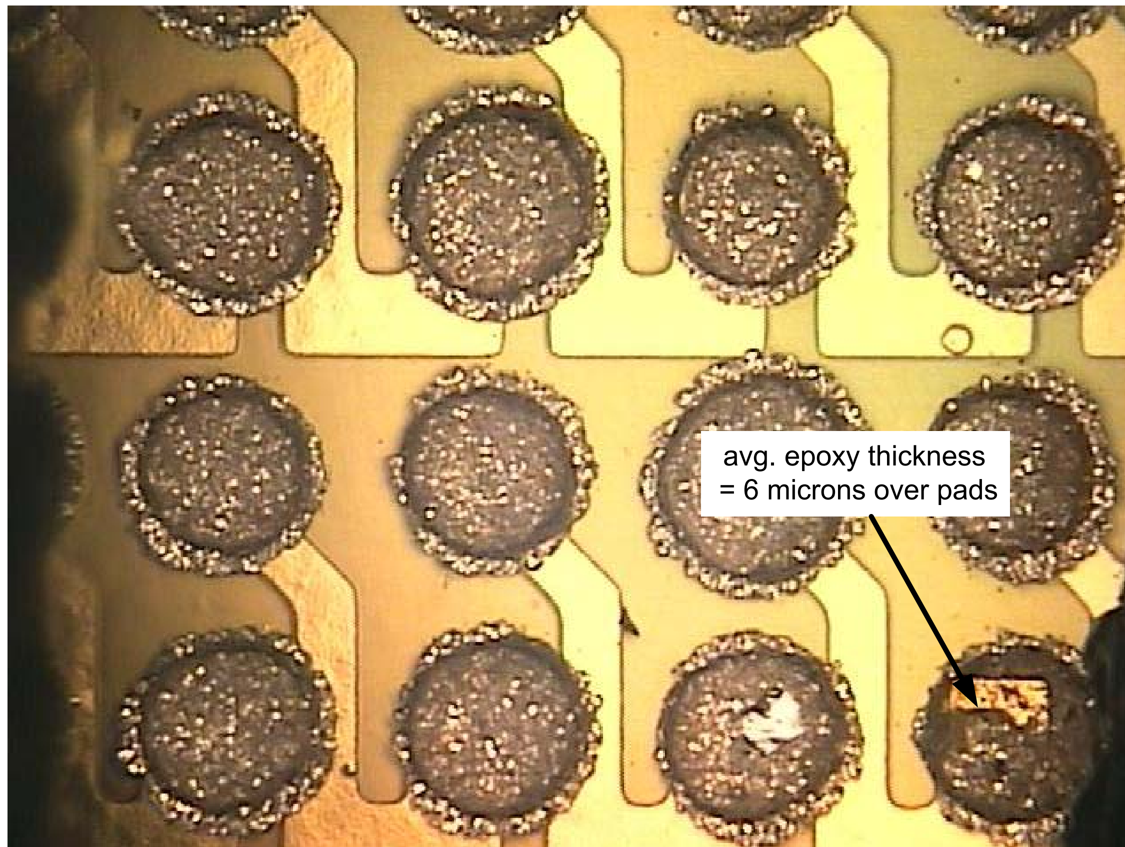
Exploded View of Polymer Bump Assembly Process



Completed Test Assembly



Conductive Polymer Bump Deposition



Single Side Deposition w/ Large Bumps

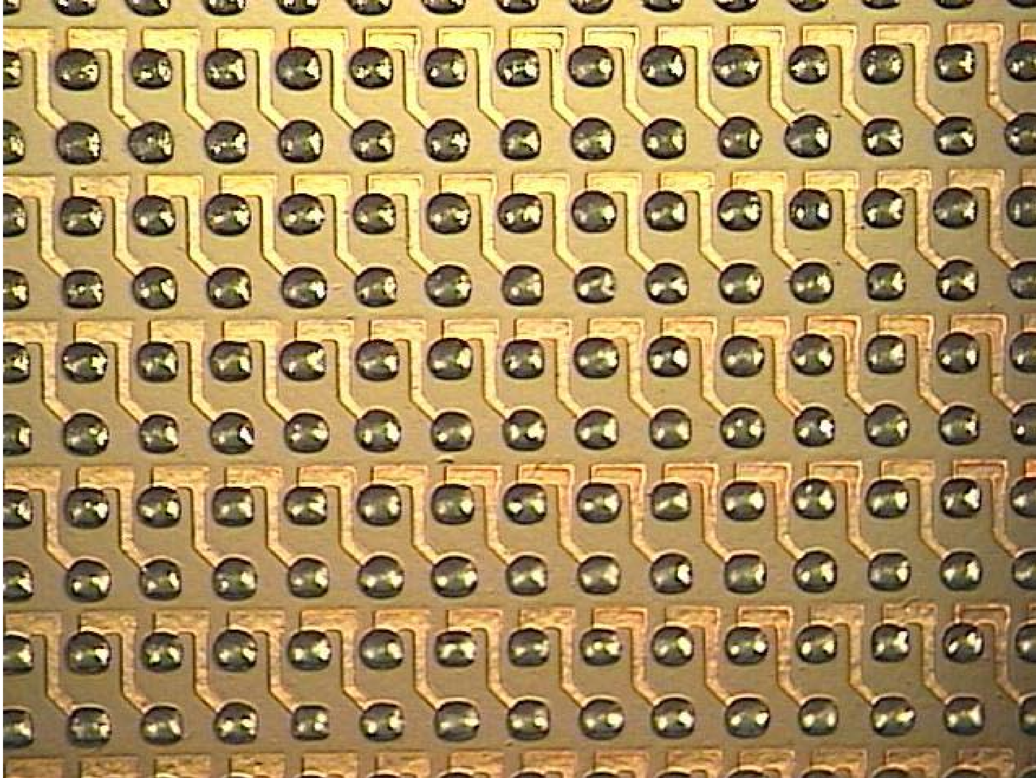
Problems:

When compressed bumps flow, causing shorts.

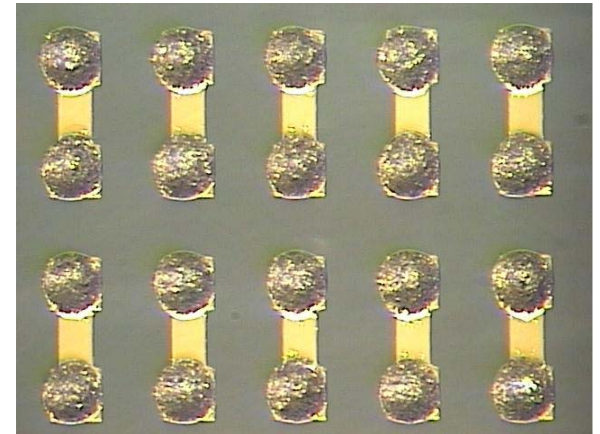
Final gap between the two substrate surfaces only 6μm wide.

(underfill not possible)

Conductive Polymer Bump Deposition



In separate 5 test runs of 2-D interconnect test structures, each w/ 8000 bumps, the yield was 100%.



Smaller Bumps Deposited on Both Surfaces

Lessons Learned and Future Directions

- **<u>Enabling technology</u>** for high-density, massively parallel signal processing electronics
- Vertical stacking of CMOS substrates works, but complex process
- Current HDI limits pixel pitch to > 75μm
- Large arrays had to be tiled using sub-modules
- Evaluating advanced stacking schemes and bonding technologies (wafer scale, automatic stacking)
  - simplify/ eliminate bump bonding (μ-wave bonding?)
  - eliminate the horizontal HDI layers
  - move from MCM-type technology to VLSI (e.g. thinned multi-layer horizontal wafer stack)

3-D Packaging Challenges

- Design evolution towards integration of sensor, electronics and packaging
- Known Good Die (KDG)
- Power dissipation
- Repairability
  - self-test
  - redundancy
  - (self)-reconfigurable